# Upgrade of the ALICE readout and trigger system Technical Design report

## **ALICE** collaboration

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# **Chapter 1**

# Introduction and executive summary

#### **1.1 Upgrade strategy**

ALICE (A Large Ion Collider Experiment) is the detector at the CERN LHC dedicated to the study of strongly interacting matter, in particular the properties of the Quark-Gluon Plasma (QGP). The ALICE collaboration plans a major upgrade of the detector during Long Shutdown 2 (LS2), which is at present foreseen to start in Dec. 2017. The scientific goals of this upgrade together with a basic description of the detector upgrade plans can be found in a Letter of Intent (LoI) [1], that was endorsed by the LHCC in September 2012.

The present ALICE detector is shown in Fig. 1.1, a detailed description of the detector can be found in [2] and the performance is summarised in [3]. ALICE will collect  $1 \text{ nb}^{-1}$ PbPb collisions before LS2, at peak luminosities of L= $10^{27} \text{ cm}^{-2} \text{s}^{-1}$ , corresponding to a collision rate of 8 kHz. Hardware triggers based on event multiplicity, calorimeter energy and track  $p_T$  provide event selectivity that allows sampling of the full luminosity. The maximum readout rate of the present ALICE detector is limited to 500 Hz of PbPb events.

The physics objective of the upgrade is aimed at precision measurements of the QGP, which will be accessible through measurement of heavy-flavor transport parameters, quarkonia down to zero  $p_T$  and low mass di-leptons. Since these processes do not exhibit signatures that can be selected by hardware triggers, they can only be collected by a zero bias (minimum bias) trigger. Additional physics topics include studies of jet quenching and fragmentations as well as study of exotic heavy nuclear states.

<sup>123</sup> The ALICE upgrade strategy is therefore based on collecting >  $10 \text{ nb}^{-1}$  of PbPb colli-<sup>124</sup> sions at luminosities up to L= $6 \times 10^{27} \text{ cm}^{-2} \text{s}^{-1}$  i.e. collision rates of 50 kHz, where *each* <sup>125</sup> *collision is shipped to the online systems*, either upon a minimum bias trigger or in a self-<sup>126</sup> triggered or continuous fashion. The Lol considers in addition the collection of 6 pb<sup>-1</sup> of

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pp collisions at the equivalent PbPb nucleon energy as well as  $50 \text{ nb}^{-1}$  of pPb collisions, 127 both at a levelled collision rate of 200 kHz. With this program the statistics for the above 128 mentioned physics topics will be increased by a factor 100 over the numbers achievable 129 with the present ALICE detector up to LS2. In order to further enhance the sensitivity to 130 charmed mesons and to make even the measurement of charmed baryons possible, an 131 upgrade of the silicon tracker with significantly increased secondary vertex resolution and 132 high standalone tracking efficiency will be implemented. Highly efficient triggering will be 133 ensured by a new interaction trigger detector. 134

<sup>135</sup> The overall goal of the ALICE upgrade therefore consists of replacing the present sili-<sup>136</sup> con tracker, upgrading the ALICE sub-detectors to read-out 50 kHz PbPb collisions and <sup>137</sup> 200 kHz pp and pPb collisions at nominal performance as well as implementing a new <sup>138</sup> online system that is capable of receiving and processing the full detector information. <sup>139</sup> Since the TPC drift time of 100  $\mu$ s is 5 times longer than the average time between in-<sup>140</sup> teractions, the presently employed gating of the TPC wire chambers must be abandoned <sup>141</sup> and continuously sensitive readout detectors using GEMs will be implemented.

The idea of reading the full detector information, either upon a minimum bias trigger or in a continuous fashion, requires one single trigger level based on an interaction trigger detector only. However, in order to keep flexibility and to allow trigger contributions for the elimination of possible background signals as well as triggers for calibration and commissioning, a Central Trigger Processor (CTP) delivering several trigger signals will be employed.

## **1.2 System upgrade overview**

The specification for the ALICE detector upgrade is set by the collision rate of 50 kHz for PbPb and a collision rate of 200 kHz for pp and pPb. The upgrade architecture is presented in Chap. 2 and in particular the Common Readout Unit (CRU) that will provide the interface between the on-detector electronics and the online computing system. As a baseline the CRU units will sit in a counting room outside the radiation area and will receive data from the detectors through optical fibers via the GBT link.

The radiation load for the upgrade program is discussed in Chap. 3. For the sensors closest to the beampipe we expect an ionizing dose up to 1 MRad and a fluence of  $10^{13}$ hadrons/cm<sup>2</sup> in units of 1 MeV neutron equivalent.

The central trigger processor (CTP) will be upgraded to accommodate the higher interaction rate, providing trigger and timing distribution (TTS) to the upgraded detectors and backwards compatibility to detectors not upgrading their TTS interface. This upgrade is described in Chap. 4.

The present Inner Tracking System (ITS) is based on two layers of Silicon Pixel Detectors (SPD), two layers of Silicon Drift Detectors (SDD) and two Layers of Silicon Strip Detectors (SSD). This detector will be replaced by 7 layers of monolithic silicon pixel detectors, as described in the ITS conceptual design report [4] and the ITS technical design report

#### 1.2 System upgrade overview

[5]. The ITS will be able to provide readout at rates of 100 kHz for PbPb and 1 MHz for pp
 collisions.

The Time Projection Chamber (TPC) is presently based on a gated readout with wire 168 chambers. The electron drift time of 100  $\mu$ s from the central electrode to the readout 169 chambers, together with the ion drift time of 180  $\mu$ s from the sense wires to the gating 170 grid, allows operation only up to about 3.5 kHz. The TPC upgrade therefore foresees the 171 replacement of the wire chambers with GEM detectors, that allow continuous operation 172 to read out 50 kHz PbPb collisions. The TPC electronics will push the digitized and time 173 stamped TPC data to the online systems in a trigger-less mode. For calibration and 174 commissioning purposes, a triggered mode of operation will be implemented as well. 175 The TPC upgrade is described in a specific technical design report [6]. 176

The readout of the TPC detector as well as the muon chambers (MCH) will be performed
by a dedicated ASIC (SAMPA) that is presently being developed. The SAMPA chip will
contain 32 channels and is based on the ALTRO and S-ALTRO developments. It will
perform analog signal shaping, 10 bit digitization at 10 MHz and digital signal processing.
The output data are presented on 320 Mbit/s serial ports. This ASIC is discussed in detail
in Chap. 5.

The Muon Chamber System (MCH) consists of a sequence of 5 wire chambers stations in the forward region of the experiment. It is presently limited to 1 kHz readout rate and will change the entire readout electronics using the SAMPA chip to digitize the detector signals. It will ship the data to the online system, either in continuous mode or upon an interaction trigger. The upgrade is discussed in Chap. 6.

The Muon Trigger detector (MTR) is at present providing the selection of high  $p_T$  single muon and di-muon events with a maximum trigger rate of 1 kHz. As the upgrade trigger strategy does not foresee a muon trigger, all events will be read upon the interaction trigger and the data are used offline for hadron rejection. Consequently the detector will be called Muon Identifer (MID). This upgrade is presented in Chap. 7.

The Transition Radiation Detector (TRD) is presently limited to a few kHz readout rate. 193 Reducing the data volume from the detector by using 'tracklets' and increasing the data 194 throughput of the off-detector electronics, a readout rate of 100 kHz for PbPb and pp can 195 be achieved. Since the front-end electronics does not support the use of multi event 196 buffers, a 100 kHz trigger rate corresponds to  $\approx$  60 % of events being read out. At 50 kHz 197 PbPb collisions  $\approx$  75 % of the events will be read-out. Going beyond this number is not 198 conceivable, because a change of the on-detector electronics would be needed, which 199 requires a removal and disassembly of all TRD modules. The TRD upgrade is described 200 in Chap. 8. 201

The readout rate of the Time Of Flight detector (TOF) is at present limited to 40 kHz by the throughput of the VME system located in the crates at the end of the detector modules. An upgrade of this element will allow TOF to readout > 200 kHz PbPb events, which easily satisfies the requirements. The TOF upgrade is described in Chap. 9.

The V0/T0/FMD detector system will be replaced by a Fast Interaction Trigger (FIT) detector, that will provide the minimum bias interaction trigger for the experiment. The FIT

detector system will be located in the forward region of the ALICE detector at positions 208 close to the present V0/T0 location. The FIT will consist of a new assembly of Cherenkov 209 and scintillator detectors with > 99 % of efficiency and < 30 ps time resolution for PbPb 210 events. The excellent time resolution is used for vertex selection with 1 cm resolution as 211 well as start time for the TOF detector. Due to its proposed granularity the detector will 212 be also able to provide event plane determination. The trigger and readout electronics of 213 this detector system resembles closely the one of the present T0 system. The detector is 214 described in Chap. 10. 215

The Zero Degree Calorimeter (ZDC) is located at a distance of 115 m from the interaction point and will change the readout electronics to triggered readout at high rate. It will provide trigger information that can be used to clean the interaction trigger, as described in Chap. 11.

The Electro-Magnetic (EMC) and Photon Spectrometer (PHO) calorimeters use the same readout electronics, which is being upgraded to 50 kHz operation already during LS1. This readout will be kept also beyond LS2 and the implementation of this system into the upgraded readout architecture is discussed in Chap. 12 and Chap. 13. The fact that not all of the 200 kHz minimum bias pp events can be read-out is not considered an issue.

The High Momentum Particle Identifier (HMP) will not be modified and will therefore be capable of reading 2.5 kHz PbPb and pp events. The implementation of this detector into the upgrade readout architecture is discussed in Chap. 14.

The Alice Cosmic Ray Detector (ACO) will not be modified, but is already capable of a readout rate of 100 kHz. The implementation of this detector into the upgrade readout architecture is discussed in Chap. 15.

The online systems will receive the full detector information. Online calibration, event reconstruction and event data reduction will allow writing all the events to tape. The online systems are briefly discussed in Chap. 2 and described in detail in a separate technical design report [7].



Figure 1.1: The present ALICE detector.

# **Chapter 2**

# Upgrade architecture

#### 237 2.1 Introduction

The general approach for the ALICE upgrade is to read out all PbPb events at the anticipated interaction rate of 50 kHz. The detector electronics and the online computing systems are designed to keep the nominal performance, even in case of noise or background larger than anticipated, and scale to twice this performance in case of higher interaction rates.

The high interaction rate and the large event size result in a data flow of  $\approx$  1 TB/s from the detectors to the on-line system. Partial event reconstruction and data reduction in the online systems results peak data rate to storage of 80 GB/s. The continuous readout of some detectors, the online calibration and the reconstruction will impose a major paradigm shift of the online and offline computing [8].

In the present system implementation ALICE provides a framework of common readout
 and trigger interfaces. The detector data link [9][10] provides a standard on-detector
 source interface unit (SIU) to connect optically to the Data Acquisition Readout Receiver
 Cards (RORC) located in the DAQ computers. The trigger and timing distribution system
 is based on the TTC architecture.

ALICE will continue and expand the approach using standard system interfaces for the 253 upgrade. The DDL will be upgraded to a higher bandwidth link and complemented with 254 a common readout unit (CRU). The CRU forms the interface between the detector links 255 and the DDL connecting to the DAQ. It also allows connection to the trigger and timing 256 distribution (TTS) network. Depending on sub detector specifications, detector data sent 257 to the CRU are multiplexed, processed and formatted. The CRU on-detector interface 258 is based on the GBT and optical versatile link [11] protocol and components. For de-259 tectors upgrading their TTS interface the central trigger processor (CTP) will provide the 260 information via the GBT protocol. For detectors not upgrading their interfaces backwards 261 compatibility to Run1 and Run2 systems is provided. 262

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## 263 2.2 System architecture



Figure 2.1: General ALICE system block digram.

Figure 2.1 shows the general ALICE readout scheme. The cavern located CTP con-264 nects to the TTS via the Local Trigger Units (LTU) which, depending on detector system, 265 are based on GBT links or the TTC [12] links. The detector front-end systems connect 266 via front-end links to either the ALICE common readout unit (CRU) or detector specific 267 readout systems. The readout systems are connected to the online computing nodes 268 (OCN) and the detector control system (DCS) via the ALICE standard optical detector 269 data link which exists in three transmission speeds (DDL1, 2, 3). Three general readout 270 configurations exist: 271

#### 2.3 Trigger system

Level	Trigger Input to CTP	Trigger output at CTP	Trigger decision at detector	contributing detectors
	[ns]	[ns]	[ns]	
LM	600	700	900	FIT
L0	1200	1300	1500	ACO, EMC, PHO, TOF, ZDC
L1	5700	5800	6000	EMC, ZDC

Table 2.1: Latency and contributors of the different trigger signals.

In one configuration the LTU uses the GBT link protocol to transmit the timing and trigger information directly to the counting room located CRUs via a trigger distribution module and the back plane of the CRU crate. The CRU modules forward the data to the detector front-end electronics via the GBT front-end links.

- The second configuration is used for detectors which need a minimum latency trigger path and also uses the CRU for the readout. The LTUs connect the TTS links based on GBT or TTC to the detector front-ends bypassing the CRU.
- The third configuration does not use the CRU to read out the detector. The detector specific readout systems use TTS links based on GBT or TTC from the LTU and connect via DDLs to the OCNs.

## 282 2.3 Trigger system

The upgraded ALICE trigger system supports the readout of triggered and continuously readout detectors. Not all subsystems will be capable of reading the full event rate. These detectors will therefore be read out whenever they are not busy. The information is merged with the data from the other sub-detectors in the online system.

The CTP will provide three trigger signals. The latencies and possible contributors to the 287 three trigger signals are shown in Tab. 2.1. The LM signal is produced by the fast interac-288 tion trigger detectors (FIT), with a latency that is compatible with the timing requirements 289 of the TRD wakeup signal. At nominal operation this is the only trigger contributor and 290 L0, L1 are simply delayed copies of the LM signal. The L0 timing is chosen such that 291 the EMC, PHO, TOF, ACO and ZDC trigger can be used as L0 contributors. The ZDC 292 allows to clean the interaction trigger in case of excessive background signals outputs. A 293 possible L1 contributor is the EMC jet trigger. The use of trigger signals by the different 294 detectors is summarised in Tab. 2.3. 295

#### 296 2.3.1 Heartbeat trigger

As the online system supports the continuous readout of detectors the event building is based on the assembly of data recorded during the a time frame of configurable length common to all detectors. In order to minimise the number of events where data are
 spread across a boundary of two consecutive time frames, the time frame duration will be
 made long compared to the TPC drift time. A value of at least 100 ms is thus foreseen.

The time frame boundaries are communicated to the detector readout electronics via transmission of non-physics heartbeat triggers allowing the separation of the data stream into pieces for the event building. The heartbeat trigger will be scheduled by the CTP to run with the highest possible priority and with a fixed period [13].

The heartbeat trigger will also be used by the detector electronics to verify whether its local bunch crossing, orbit and trigger counters are still synchronized. Each readout unit will generate an empty heartbeat event when receiving the corresponding trigger. These events will be used by the online systems for data segmentation, fault finding and recovery procedures. The detector electronics of the existing detectors will be modified to handle this combination of physics and heartbeat triggers.

Each readout card will autonomously tag the data using the local copy of the LHC Orbit and the bunch crossing id (BCID). For continuous readout the data will be sent as a continuous flow of successive time frames each preceded with a header containing the time-based tagging. A trailer indicates error cases such as data truncation due to the early arrival of a physics or heartbeat trigger. The triggered readout will function in the same way as it is presently the case: it will send a data block preceded with a header for every trigger, physics or heartbeat.

Figure 2.2 shows how the physics and heartbeat triggers will be used for the continuous and triggered readout.



Figure 2.2: The usage of physics and heartbeat triggers for the continuous and triggered readout.

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#### 2.3.2 Trigger, Timing and clock distribution System - TTS

Depending on the detector implementation, whether the trigger latency is critical and whether the TTS interface is upgraded, three different TTS configurations are implemented. The distribution system for the upgraded detectors is based on GBT links between the CTP and the readout electronics. For non-trigger latency critical systems, such as the TPC and MCH systems, the TTS connects the CTP to the off-detector readout electronics. The off-detector electronics takes care of distributing the trigger and timing

#### 2.4 ALICE Detector Data Link - DDL

signals to the front-end electronics. In case of latency critical systems, such as the ITS,
 the TTS connects the CTP directly to the on-detector electronics via optical GBT links.
 Those systems which do not upgrade their TTS interface will continue to use the TTC
 chip set. As a consequence the upgraded CTP will offer two interfaces, one based on the
 GBT protocol and one based on the TTC protocol.

The bandwidth of the TTS based on GBT is sufficiently high to transmit for each trigger 333 (physics, software or heartbeat) the full trigger and timing information. The present TTC 334 system used to distribute these messages has a saturation rate of its B-channel used for 335 the distribution of trigger signals which depends upon the length of the trigger message: 336 150 kHz for 8 words message and 225 kHz for 6 words messages. A reliable usage of 337 the B-channel imposes a limit on the trigger rate to half of these values which will not 338 allow distributing the full information for each trigger. Detectors which will continue the 339 use of the TTC system will receive for each trigger shortened information via the TTC B-340 channel. In the detector front-end electronics local copies of the BCID, the orbit counters 341 and trigger counters are implemented, which are independently increased and attached 342 to the data packets. The arrival of the heartbeat trigger with the full trigger information 343 allows counter re-synchronisation and, if required, error flagging. 344

### 345 2.4 ALICE Detector Data Link - DDL

The present ALICE data collection is based on common interfaces between the detector readout electronics and the online computing systems: the Detector Data Link (DDL1) [9]. A second version of the link (DDL2) has been developed [10] and will be used by the TPC and TRD detectors during Run2. For the upgrade a higher performance readout solution will be developed. The interface with the online system will be based on the DDL3 or an input-output slot of a PC.

The three generations of DDLs have different clocking speed and form factors. The 352 DDL1 is clocked at 2.125 Gb/s and the DDL1 Source Interface Unit (SIU) is implemented 353 as a radiation-tolerant daughter card plugged on the detector readout card. The DDL2 354 SIU is implemented as an Intellectual Property (IP) core and can be clocked at 4.25 or 355 5.3125 Gb/s according to the capabilities of the detector electronics including it. The 356 DDL3 aims at higher bandwidths using Gigabit Ethernet at 10 or 40 Gb/s or Infiniband 357 (IB) at 56 Gb/s. The performance of the DDL1, of the two variations of the DDL2 and of 358 a first DDL3 prototype based on Ethernet are shown in Fig. 2.3. 359

### **2.5 The Common Readout Unit - CRU**

The CRU acts as the interface between the on-detector systems, the online computing nodes (OCN) and the central trigger processor (CTP). It is based on high performance FPGA processors equipped with multi gigabit optical inputs and outputs. The interface to the detector control system (DCS) is done via the DAQ OCN or via a commercial network



Figure 2.3: The performance of the DDL1 clocked at 2.125 Gb/s, of the two variations of DDL2 clocked at 4.25 and 5.3125 Gb/s and of a prototype of DDL3 clocked at 10.3125 Gb/s.

switch. A block diagram of this system is shown in Fig. 2.1. Where possible the new
 detectors or those for which the electronics is redesigned will be read out by the CRU.

Bi-directional front-end links based on the Versatile Link [11] and the GigaBit Transceiver (GBTx) serializer/deserializer chip connect the on-detector systems to the counting room located CRU carrying hit data, configuration and trigger information. Depending whether the automatic SEU error correction is activated the link bandwidth is 3.2 Gb/s or 4.48 Gb/s.

Bi-directional DDLs connect the CRU to the DAQ OCNs carrying hit data and configuration data. The DDL is implemented either as DDL3 or as a slot of the input-output bus of a PC (PCIe Gen 3). Presently for all system and cost considerations a DDL bandwidth of 10 Gb/s is assumed.

The GBT based trigger and timing distribution (TTS) links connect the CTP to the CRU which forwards the trigger data to the on-detector electronics. For some detectors the TTS links transport the busy signal from the CRU to the CTP. For most detectors the CRU only multiplexes the data from several front-end links into more performant high speed data links without any data processing. The TPC is one exception, where the CRU re-orders the data samples according to their position in the pad row allowing a more efficient cluster search in the OCNs.

An alternative approach has been investigated, where the CRU is located in the cavern 383 and electrical front-end links connect the detector to the CRU. 10 GbE interfaces on long 384 fibers connect the CRU to the DAQ computer on comparatively lower number of links due 385 to the superior link bandwidth. For the TPC and ITS these units would sit directly on the 386 ALICE detector and thus need to be tolerant to radiation. The CRU would be based on 387 comparatively low performance radiation tolerant FPGA design. However, in this case 388 one needs to consider the limited access during LHC operation, the difficult installation 389 and maintenance, the required radiation tolerant design and verification campaigns. 390

#### 2.5 The Common Readout Unit - CRU

In summary, from system level point of view, the GBT based CRU located outside of
 the detector presents a more robust and clean system with more processing power and
 flexibility towards future requirements with a lower impact on the cavern infrastructure.
 Consequently the CRU-counting room option is pursued. For a more detailed evaluation
 and cost comparison refer to [14].

The ALICE CRU system evaluation is based on the hardware implementation basis of 396 the AMC40/TELL40 system developed in the framework of the LHCb readout [15]. The 397 system is based on the ATCA crate standard. One ATCA carrier board houses 4 ad-398 vanced mezzanine cards (AMC40) each with up to 36 optical bi-directional links with a 399 bandwidth of up to 10 Gb/s per link. Fig. 2.4 shows a picture of the mezzanine card. 400 Figure 2.5 shows a block diagram of one mezzanine card. In the standard application 401 24 of the bi-directional optical connections are used to connect 24 GBT front-end links, 402 carrying detector data to the CRU and transmitting configuration and optionally trigger 403 data to the on-detector electronics. The DDL3 links use the remaining 12 bi-directional 404 connections to forward the hit data to the online computing system and send configura-405 tion data to the CRU. Cost calculations, as shown in the detector descriptions are based 406 on this configuration. In some applications the number of links between the online com-407 puting nodes and the CRU can be reduced, allowing a higher number of front-end links to 408 be connected. Also other similar concepts are taken into consideration, such as the MP7 409 system developed for CMS [16]. 410



Figure 2.4: AMC40 ATCA mezzanine card. The front-panel contains 36 optical inputs and 36 optical outputs.

For the CRU system implementation next to the TCA crate configuration a solution where the CRU is plugged directly into PCIe slot of the online computing node is evaluated. In that case the PCIe bus serves as DDL3. However, in this configuration the CRU output data bandwidth needs to be decreased to the PCIe bandwidth requiring more CRU boards and the trigger distribution cannot be done on the crate back plane. Furthermore with the evolution of PCIe bus long term compatibility might be an issue. Consequently a crate based CRU solution is considered as base line for the CRU implementation.

The present version of the AMC40 system can accommodate FPGAs which are available with three matrix sizes. Presently all prototypes have been equipped with FPGAs of the smallest size. Should it turn out that the matrix size is insufficient for applications, where data processing on top of the data multiplexing is performed, the two larger pin compatible FPGAs can be used with the same printed circuit board. Cost estimates and performance estimates have been done taking the smallest FPGA into account.

The GBT links support forward error correction allowing the correction of transmission 424 errors due to single event upset effects, however, reducing the data bandwidth from 4.48 425 Gb/s to 3.2 Gb/s. Fig. 2.6 shows a block diagram containing the main building blocks in 426 the CRU system based on GBT front-end links. Electrical serial e-links [11] with a length 427 of a few meters connect to the GBTx e-link interface. Each e-link contains a bi-directional 428 data link and a clock output. Depending on operation mode the GBT protocol allows 429 a bit rate setting of 320, 160 or 80 Mbit/s and offers 10, 20 or 40 e-links respectively. 430 This allows the adaptation of the e-link data rate to the detector application. For instance 431 the TPC with its high data volume will operate in the 320 Mbit/s mode where only 10 432 e-links are available for one GBT optical link. The muon chamber detector (MCH) will 433 use the link at 80 Mb/s as the data rate per front-end unit is much lower in order to profit 434 most efficiently from the GBT data bandwidth. The GBTx ASIC decodes the data and 435 transmits it via the versatile optical link components. Two different types of components 436 are available. The VTRx is a radiation hard optical transceiver component offering one 437 input and one output. The VTTx is a double optical transmitter. These two components 438 allow convenient adaptation of the readout bandwidth to the detector segmentation. For 439 example in the TPC system, which has many more data links to the CRU than TTS 440 links to the detector, the VTTx component is used for the front-end links and the VTRx 441 component for the fewer TTS links. The MCH has as many front-end links as TTS links 442



Figure 2.5: CRU block diagram.

#### 2.5 The Common Readout Unit - CRU

and thus will use only the VTRx component. A dedicated slow control adapter (SCA)
 ASIC [17] provides I2C interfaces to transmit the configuration data to the detector front end, as well as ADCs to verify the supply voltages and DACs to provide bias.



Figure 2.6: System block diagram with GBT and versatile link chip set.

In the TPC, MCH and MID the trigger latency is not critical and thus one can afford to send 446 the trigger data from the CTP in the cavern to the CRU in the counting room and from 447 there to the detector. Assuming a maximum cable length of twice 150 m an additional 1.5 448  $\mu$ s of latency applies. It should be noted that using constant latency GBT links from the 449 CTP to the CRU and again from the CRU to the FEC the trigger information will arrive 450 with constant latency at the front-end. Using a TCA crate solution for the CRU has the 451 advantage that the trigger and timing information can be distributed via the high speed 452 back plane and thus the number number of trigger links from the local trigger units (LTU) 453 to the CRU is very low, see Tab. 4.3. 454

The ITS plans for 976 1 Gb/s electrical front-end links leaving the detector staves, which extend to ITS 184 readout cards located in the mini frame. These cards multiplex the ITS front-end link protocol into either the GBT compatible format or directly to the DDL3 format. Due to maximum latency restrictions the trigger signal must be routed directly from the CTP to the detector without a detour via the counting room and thus the TTS interface needs to be located on the ITS readout card.

The ALICE collaboration has two institutes responsible for the ALICE CRU design. The 461 Wigner Institute, Hungary, is the institute, which developed and produced the previous 462 version of common readout developments, the DDL1 and DDL2, as well as the ALICE 463 Data Acquisition Readout Receiver Cards version D (D-RORC). The version of the RORC 464 (D-DORC) was designed by the university Frankfurt and produced by the Wigner institute. 465 These cards are already PCIe bus plug-in cards, see Fig. 2.7 and 2.8. The CRU based on 466 ATCA or PCIe is an evolution of the existing developments. The second institute involved 467 is the Variable Energy Cyclotron Centre, VECC, India. The development will be carried 468 out in collaboration with other experiments. 469

Presently from technical stand point the afore mentioned AMC40 solution and also the
 CMS developed MP7 are following a similar approach, where high performance FPGAs
 together with multi channel gigabit transceivers are housed in a microTCA crate. Both

the AMC40 and MP7 system development is advanced and full prototypes are available for evaluation.

### **2.6 Readout of detectors not using the Common Readout Unit**

Those detectors, which do not use the CRU, will use detector specific back-end electronics, which interface to the ALICE OCNs via the DDL1 or DDL2.

Table 2.2 summarises the DDL, CRU FE and TTS-FE link usage detector by detector.
DDL links connect to the Online Processing Nodes (OCN). CRU-FE-links carry hit data
from the on-detector electronics to the CRU. TTS-FE links carry trigger data from the
CRU to the on-detector electronics, see Fig. 2.6. Detectors with 0 TTS-FE links use the
CRU but receive the TTS information directly from the CTP at the on-detector electronics.
Detectors with no entries for TTS-FE links do not use the CRU.

Detector	DDL1	DDL2	DDL3	CRU-FE-links	TTS-FE links
	2.125 Gb/s	4.25-5.3125 Gb/s	10Gb/s	3.2 Gb/s	3.2 Gb/s
TPC			1836	6336	1764
MCH			250	500	500
ITS			60*	184 *	0
MID			8	16	16
ZDC			1	1	
TOF		72			
FIT		1			
ACO	1				
TRD			36	1044	0
EMC		20			
PHO		16			
HMP	14				
Total	15	109	2191	8081	2280

 Table 2.2: Number of DDL, CRU-front-end links and TTS-FE links. (\* depending on implementation the ITS on-detector electronics will either use DDL3s to connect to the OCNs or CRU data FE-links to the CRU. Numbers shown reflect the CRU configuration.)

## **2.7** Data framing, aggregation and event building

The global architecture of the online system as presented in the upgrade Lol [1] is shown in Fig. 2.9.

Each detector will split its data over several DDLs to accommodate their segmentation and readout rate. The architecture foresees that online computing nodes (OCN) collects

#### 2.8 Detector overview

the data of the DDLs. For detectors using the DDL3 it is planned that 10 DDL3s corresponding to a bandwidth of 100 Gb/s are matched with 3 slots of the most common I/O bus presently available in the PCs, the PCI Express Generation 3 with 8 lanes.

Data (delimited by consecutive heartbeat events) will be assembled in two stages. The 492 time frames delivered by the DDLs connected to each OCN will be assembled together 493 on the basis of the time stamping. A first stage of reduction of the data volume will be 494 applied in the OCN performing local data processing e.g. cluster or tracklet finder. Event 495 Processing Nodes (EPN) perform the second level of data aggregation and a further 496 reduction of the data volume will be applied in the EPN by performing a global processing 497 allowing for example to reconstruct the tracks and associate them to their primary vertex. 498 This will allow to disentangle the different interactions included in a timeframe and to 499 perform the event building. 500

### **501** 2.8 Detector overview

For the detector readout system implementation the introduction of the heartbeat trig-502 ger and the bandwidth limitations of the TTC system requires all detectors to implement 503 copies of the bunch crossing, orbit and trigger counters. The hardware needs to compare 504 these counters with the LHC counters which are only transmitted in full during a heartbeat 505 event. In case of a discrepancy the detector electronics needs to re-align the counters 506 and communicate the error to the DAQ system. Furthermore for the upgrade the CTP 507 will allow interleaved trigger sequences, where several L0 signals can be sent before the 508 corresponding L1 signals will arrive. Detector systems will implement or upgrade their 509 trigger interface accordingly. 510

Table 2.3 shows a summary the sub-detectors with respect to their integration in the readout system. Horizontal lines separate detectors with similar readout properties. The first group supports triggered readout and continuous readout. The second group needs a trigger, but has sufficient multi event buffer capability so that when read out at design rate no dead time occurs. The last group has insufficient multi-event buffering and will not have dead time free operation.

Table 2.4 shows the number of channels in the system and the components to be replaced for the upgrade. Details are discussed in the corresponding sub-detector section.

Det	triggered by	design RO	busy	TTS	CRU used
	() = optional	rate [kHz]	[%]	GBT/TTC	
TPC	(L0 or L1)	50	0	GBT	у
MCH	(L0 or L1)	100	0	GBT	У
ITS	LO	100	0	GBT	У*
MID	L0 or L1	>100	0	GBT	У
ZDC	L0	>100	0	GBT	У
TOF	L0 or L1	100	0	GBT	n
FIT	L0 or L1	100	0	GBT	n
ACO	L0 or L1	100	0	TTC	n
TRD	LM&L0 or L1	50	25	GBT&TTC	У
EMC	L0&L1#	46	100	TTC	n
PHO	L0&L1#	46	100	TTC	n
HMP	L0&L1#	2.5	100	TTC	n

 Table 2.3: Readout parameter overview. (\* depending on implementation the ITS on-detector electronics will either use DDL3s to connect to the FLPs or GBT data FE-links to the CRU. (# these detectors need L0 and can optionally L1.

Det	# of channels	FE ASIC	FEC	MUX
TPC	<b>5</b> *10 <sup>5</sup>	17 k SAMPA	3400	CRU
MCH	$10^{6}$	33 k SAMPA	500	CRU
ITS	<b>25*</b> 10 <sup>9</sup>	25k pixel	200	CRU
TOF	<b>1.6</b> *10 <sup>5</sup>			72 DRM
MID	<b>21</b> * 10 <sup>3</sup>	FEERIC	234	CRU
FIT	160+64		upgrade	DRM(TOF)
ZDC	22		commercial&1 ZRC	CRU
TRD	<b>1.2</b> * 10 <sup>6</sup>			CRU
EMC	<b>18 *</b> 10 <sup>3</sup>			
PHO	<b>17</b> * 10 <sup>3</sup>			
HMP	<b>1.6</b> *10 <sup>5</sup>			

 Table 2.4: Upgrade effort. (FEC..front-end controller, first data concentration stage, MUX..data multiplexer, second data concentration stage and interface to OCNs.



Figure 2.7: ALICE C-RORC.



Figure 2.8: ALICE D-RORC.



Figure 2.9: The global architecture of the online system.

# **Chapter 3**

# **Radiation environment**

Radiation calculations for the present ALICE detector, performed with FLUKA [18] and the 521 VMC interface [19], can be found in [20]. In this chapter, updated calculations that take 522 into account the recent results on measured multiplicities for PbPb, pp and pPb collisions, 523 are presented. The hadron fluence, quoted in 1 MeV neutron equivalents (neg), and the 524 Total lonising Dose (TID) are the numbers that determine the long term radiation damage 525 of sensors and electronics. The two numbers are given in Figs. 3.1 and 3.2 for a delivered 526 PbPb luminosity of 10 nb<sup>-1</sup>. The rate of hadrons with a kinetic energy > 20 MeV passing a 527 given area determines the rate of single event upsets in the microelectronics circuitry and 528 is given in Fig. 3.3 for 50 kHz PbPb collision rate. The simulated geometry still assumes 529 the present ITS detector with detailed implementation of services and support structures. 530 Since the upgraded ITS will use ultra light structures optimized for minimum material 531 budget, one can assume that the upgraded ITS will represent less material than the 532 present one and therefore the obtained numbers present a worst case scenario. 533

At positions with -100 < z < 350 cm, the radiation numbers are dominated by primary tracks originating from the interaction point. At z < -100 cm the frontabsorber is absorbing hadrons that are pointing towards the muon system, which leads to a decrease of the TID but an increase of the hadron fluence due to the lateral escape of neutrons from the absorber.

The planned 6 pb<sup>-1</sup> pp collisions and 50 nb<sup>-1</sup> pPb collisions are adding 13% to the TID and hadron fluence numbers. To accommodate for uncertainties in simulation, background levels and possible future physics programs we assume a safety factor of 10 on top of the simulated numbers for TID and 1 MeV neq hadron fluence. A safety factor of 2 is applied to the instantaneous rate of kinetic energy  $E_k > 20$  MeV hadrons. Table 3.1 gives the results for specific locations inside the ALICE detector. In case a range of *z*-positions is indicated, the table refers to the maximum value inside this interval.

The ITS and MFT detectors have to stand a TID close to 1 MRad and a hadron fluence up to  $10^{13}$  cm<sup>-2</sup>. The flux of high energy hadrons is close to 1.6 MHz/cm<sup>2</sup> for these detectors. The radiation levels for the FIT detector are a factor 3-4 lower but still of similar

519

Element	r	Z	TID	1 MeV neq	>20 MeV had.
	(cm)	(cm)	(kRad)	$(cm^{-2})$	$(kHz/cm^2)$
ITS L0	2.2	[-13.5, 13.5]	646	$9.2 \times 10^{12}$	1600
ITS L1	2.8	[-13.5, 13.5]	387	$6.0 \times 10^{12}$	1000
ITS L2	3.6	[-13.5, 13.5]	216	$3.8 \times 10^{12}$	500
ITS L3	20	[-42.1, 42.1]	13	$5.2 \times 10^{11}$	28
ITS L4	22	[-42.1, 42.1]	9	$5.0 \times 10^{11}$	24
ITS L5	41	[-73.7, 73.7]	6	<b>4.6</b> $\times 10^{11}$	10
ITS L5	43	[-73.7, 73.7]	4	<b>4.6</b> $\times 10^{11}$	9
MFT D0	2.5	-50	395	$6.7  imes 10^{12}$	1100
MFT D1	2.5	-58	392	$6.4 \times 10^{12}$	1040
MFT D2	3.0	-66	767	$5.9 imes 10^{12}$	760
MFT D3	3.5	-72	427	$4.3 \times 10^{12}$	520
MFT D4	3.5	-76	541	$4.8  imes 10^{12}$	560
FIT1	5	-80	181	$3.0 \times 10^{12}$	280
FIT2	5	340	103	$1.4 imes 10^{12}$	200
TPC In	79	[-260, 260]	2.1	$3.4 \times 10^{11}$	3.4
TPC Out	258	[-260, 260]	0.3	$5.2 \times 10^{10}$	0.7
TRD	290	[-390, 390]	0.4	<b>4.8</b> $\times 10^{10}$	0.54
TOF	370	[-370, 370]	0.13	$2.6 \times 10^{10}$	0.26
EMCAL	430	[-340, 340]	0.06	$1.5 \times 10^{10}$	0.02
MCH S1	19	-536	0.42	$4.2 \times 10^{11}$	3
MCH S2	24	-686	0.19	$1.4  imes 10^{11}$	1
MCH S3	34	-983	0.14	$1.6  imes 10^{11}$	0.9
MCH S4	45	-1292	0.18	$3.0 \times 10^{11}$	1
MCH S5	50	-1422	0.91	$2.5 \times 10^{11}$	0.7
CTP Rack	600	-1295	<b>4.8</b> $\times 10^{-3}$	<b>7.8</b> $\times 10^{9}$	0.03

Table 3.1: Total lonizing Dose (TID) and 1 MeV neq hadron fluence for  $10nb^{-1}$  PbPb +  $6pb^{-1}pp$  + $50nb^{-1}pPb$  collisions (including a safety factor 10) as well as high energy hadron fluence for 50 kHz PbPb<br/>collisions (including a safety factor 2).

#### 3 Radiation environment

magnitude. The TPC electronics located at the inner radius of the service support wheel
has to stand a dose of 2.1 kRad and 3.4 kHz of high energy hadrons. For muon station
1 the radiation levels are very similar, so these numbers set the scale for the radiation
tolerance of the common TPC/MCH readout chip, SAMPA.

It must be noted that the above numbers for TID and 1 MeV neq fluence are only up to a factor of 2 higher than the numbers in [20] that were originally assumed for the ALICE design, because of different assumptions on multiplicity and running conditions. The above numbers for  $E_k > 20$  MeV hadron fluence are only up to a factor of 3 larger than the ones originally assumed. The electronics of TRD, TOF, EMCAL, PHOS and HMPID, that will remain unchanged after LS2, will therefore still be well suited for the ALICE upgrade.



**Figure 3.1:** Total Ionizing Dose for an integrated PbPb luminosity of  $10 \text{ nb}^{-1}$  in the ALICE central barrel.



Figure 3.2: Hadron fluence for an integrated PbPb luminosity of 10 nb<sup>-1</sup> in the ALICE central barrel.



Figure 3.3: Rate of hadrons with energy of >20 MeV for a PbPb collision rate of 50 kHz.

# **Chapter 4**

# **Central Trigger Processor - CTP**

#### 562 4.1 Introduction

The Central Trigger Processor (CTP) will manage a system of detectors with different properties as shown in Tab. 4.2. The majority of detectors which will read out the nominal interaction rate are dead time free. However, in order to provide backwards compatibility to detectors not being upgraded, the trigger system must cope with detectors which will have dead time during the readout.

The strategy for selecting events for readout will be different from that employed in previous runs. Previously, despite the fact that ALICE events are highly complex, the trigger strategy was to combine a Minimum Bias sample with a sample selected according to thresholds in high  $E_t$  (calorimeter triggers), high  $p_t$ , or high multiplicity [2].

The interaction rates will increase to  $\approx$  50kHz for PbPb, and 200 kHz for pp and pPb [1]. Where feasible a safety margin of 2 is applied in the system design. The strategy for the upgraded ALICE system is to select and read out all interactions and apply an online data reduction in the online computing system. To achieve this, the combination of triggerless readout and a minimum bias trigger based on the new forward FIT detector is used. A few additional inputs allow for cosmic triggers and calorimeter based triggers to enhance rates for some types of events where the minimum bias trigger is inefficient.

### **4.2 Trigger architecture**

The overall system architecture is shown in Fig. 4.1. Trigger inputs are collected to satisfy three different latencies, given three different levels shown as LM, L0 and L1. The times, calculated relative to the time of the interaction, are given in Tab. 4.2.

560

Det	triggered by	design RO	busy	TTS	CRU used
	() = optional	rate [kHz]	[%]	GBT/TTC	
TPC	(L0 or L1)	50	0	GBT	у
MCH	(L0 or L1)	100	0	GBT	У
ITS	LO	100	0	GBT	У*
MID	L0 or L1	>100	0	GBT	У
ZDC	LO	>100	0	GBT	У
TOF	L0 or L1	100	0	GBT	n
FIT	L0 or L1	100	0	GBT	n
ACO	L0 or L1	100	0	TTC	n
TRD	LM&L0 or L1	50	25	GBT&TTC	У
EMC	L0&L1#	46	100	TTC	n
PHO	L0&L1#	46	100	TTC	n
HMP	L0&L1#	2.5	100	TTC	n

 Table 4.1: Readout parameter overview. (\* depending on implementation the ITS on-detector electronics will either use DDL3s to connect to the FLPs or GBT data FE-links to the CRU. (# these detectors need L0 and can optionally L1.

Level	Trigger Input to CTP [ns]	Trigger output at CTP [ns]	Trigger decision at detector [ns]	contributing detectors
LM	600	700	900	FIT
L0	1200	1300	1500	ACO, EMC, PHO, TOF, ZDC
L1	5700	5800	6000	EMC, ZDC

 Table 4.2: Latency and contributors of the different trigger signals.
#### 4.3 Central Trigger Processor

The LM latency is the same as in Run2, and is suitable for generating a wake-up signal 583 for the TRD electronics. The LM trigger will be provided by the FIT detector. The latency 584 of the LM signals is 600 ns and has three components: signal propagation from detector 585 to FEE ( $\approx$  250 ns); signal processing ( $\approx$  150 ns); propagation of processed signal to the 586 CTP ( $\approx$  200 ns). However, it will not be possible to generate a trigger signal from the 587 electromagnetic calorimeter (EMC) early enough for this trigger level, and for this reason 588 level L0 signal is retained. The ZDC is optionally available to clean the minimum bias 589 trigger provided by the FIT. The FIT detector is not suitable for cosmic ray triggers. In this 590 case TOF and ACO will be used. 591

As in the present system trigger decisions are transmitted from the CTP to the individual 592 detectors using an upgraded Local Trigger Unit (LTU). Owing to the reduced number 593 of trigger inputs with respect to Run1 and Run2, for the upgrade it will be possible to 594 implement a lookup-table trigger, allowing full flexibility in the specification of trigger logic. 595 However, due to the triggerless strategy, there will be relatively few trigger *classes* [21], 596 with most events selected by a Minimum Bias trigger with subsequent data reduction in 597 the online computing system. The selection of readout detectors will be different from 598 previous runs. Previously, a trigger was successful only if every one of a list of readout 599 detectors was available to read out the data (the list defining a trigger "cluster"). For 600 the upgrade, if a trigger condition is satisfied, the event is read out with the full set of 601 continuous readout detectors, plus all other available detectors. This strategy in effect 602 treats each detector as a separate cluster, so any combination of detectors could be read 603 out for a given event. At the same time the BUSY requirements of every detector can be 604 treated independently of other detectors and interleaving of triggers from different levels 605 is allowed where possible. It could turn out that this strategy would lead to insufficient 606 numbers of events being read out with useful combinations of detectors, for example TRD, 607 TOF and HMP, which are all used for particle identification. To allow for this possibility, 608 the trigger logic can in addition define further clusters consisting of groups of detectors, 609 as at present, and will balance the bandwidth between a free selection of all available 610 detectors and a restricted choice requiring a given combination. 611

### **4.3 Central Trigger Processor**

The functions discussed in the previous section can be implemented in a new CTP board combining the functions of the current CTP BUSY, L0, L1 and FO boards. This obviates the need to transfer data across the backplane and therefore eliminates the CTP dead time. The board incorporates the XILINX-7-series KINTEX FPGA, provided with sufficient memory to reproduce and extend the snapshot facilities of the current CTP. In particular the CTP will be provided with 1 GB of DDR3 memory, partitioned so as to allow adequate storage of snapshot data, with reserved space for future applications.

The XILINX-7 series also provides a facility for automatic recovery from radiation induced single and double event upsets for configuration. It is self-correcting after a CRC check. Since the CTP will be placed in a site of only moderate radiation (see Table 3.1), this automatic recovery procedure is sufficient for the CTP operation [22].



Figure 4.1: ALICE system block diagram.

The board will have a 10 Gb/s optical ethernet link to the DAQ, using the UDP protocol, for transmission of interaction records and trigger data, and a second 1 Gb/s optical ethernet link to DCS for configuration, control and monitoring, using the IPbus protocol. Interaction records consist of a series of record listings each orbit and the interactions which occur in it. The trigger data for every L0 and L1 trigger consist of event identification, trigger class mask and detector mask.

The CTP will also communicate with up to 24 Local Trigger Units (LTUs), one for each
 ALICE detector, using custom high speed serial links. The LTU is described in the next
 section.

# **4.4 Local Trigger Unit - LTU**

The Local Trigger Unit combines the functions of transmission of trigger signals and em-634 ulation of the CTP for use in detector development, in a way similar to that implemented 635 in the current LTU [23]. The LTU (Fig. 4.2) will have the possibility to send trigger signals 636 to detectors via the GBT or the TTC protocol. For the GBT there will be ten separate 637 bi-directional GBT links which can also be used for upstream BUSY collection. In the 638 TTC case the LTU optical links will provide the optical signal according to TTC protocol 639 and BUSY is propagated by dedicated LVDS cables. In addition there will be provision 640 for clock, orbit and external trigger inputs. Monitoring and control will be provided by a 641 1Gb/s optical Ethernet link using the IPbus protocol. 642

# 4.5 Trigger and Timing distribution System - TTS

Three different types of links are used for trigger distribution. The LM trigger level is distributed by a copper LVDS cable to the TRD, satisfying the low latency requirement. As can be seen from Tab. 4.1, two basic types of link will be used for the transmission of trigger signals and data at L0 and L1 levels. Detectors upgrading their TTS interface will use GBT links [11], while the other detectors continue to use the TTC system.

### 649 4.5.1 TTS via GBT

<sup>650</sup> The synchronous trigger signals at L0 and L1 levels will be followed by a trigger message <sup>651</sup> containing event identification, trigger class mask and detector mask.

With respect to the distribution links, the detectors using the GBT protocol are considered individually, as there are several distinct cases, as shown in Tab. 4.3. For the TPC, MCH, MID and ZDC the distribution of trigger signals will use the CRU. The reception of trigger signals is not time-critical. The design of the system implies that under nominal operation conditions it does not get busy. The detector only gets busy in case of an error condition or

### **Central Trigger Processor - CTP**

Detector	TTS links	type	Position of CRU
TPC	7	active GBT	CR
MCH	1	active GBT	CR
ITS	184	passive GBT	Cav
MID	1	active GBT	CR/Cav
ZDC	1&1	active GBT	CR & Cav
TOF	72	passive GBT	Cav
FIT	1	active GBT	CTP area
TRD	1	active GBT & TTC	CR/Cav
EMC	1	TTC	Cav
PHO	1	TTC	Cav
HMP	1	TTC	Cav
ACO	1	TTC	Cav

Table 4.3: TTS-GBT connections to detector systems. CR stands for Counting Room and Cav for Cavern.

during operation under non-nominal conditions. Thus the BUSY transmission is not timecritical and generating the BUSY signal at the level of the CRU is sufficient. Consequently bi-directional GBT based trigger links connect the CTP with the counting room located CRU. Table 4.3 shows the number of required TTS links. Even for the TPC seven links only are needed, which corresponds to the number of TCA crates estimated.

The trigger latency of the ITS detector is time critical. In this case a propagation detour via the counting room is avoided by directly routing the links from the CTP to the 184 miniframe located ITS readout boards. The unidirectional ITS trigger links are fanned out passively using optical splitters. Each LTU has 10 optical outputs and when combined with 1:32 optical splitters, a sufficient number of links is provided to cover the distribution of signals to all ITS readout boards. The busy signal transmission is done via the data links.

TRD front-end electronics still uses a trigger interface based on TTC, whereas the CRU
 based readout electronics uses GBT based TTS links. TOF and FIT will upgrade the TTS
 interface to GBT links.

### 672 **4.5.2 TTS via TTC**

The restricted bandwidth of the TTC B-channel dictates the format for the transmission 673 of trigger signals and data. While in runs 1 and 2 the bulk of the trigger data was trans-674 mitted to each TTC destination as a broadcast message in the B-channel, the increased 675 interaction rate in the upgraded system means that this strategy would lead to excessive 676 delays before the data could be transmitted. Instead, a synchronous trigger in the A-677 channel will be generated and only the 12 least significant bits of event identification will 678 be transmitted in the B-channel, asynchronously. The full trigger data will be transferred 679 as CTP readout, and attached to the data at the event-building stage. To provide the L0 680 and L1 signals, the A-channel will be coded, L0 corresponding to binary 10 and L1 to 11 681



Figure 4.2: Connections for LTU unit. sA,sB - scope outputs. TA,TB - TTC A- and B-channel outputs. ORB - orbit input, BC - clock input, ExT - external trigger input.

transmissions, thus not allowing two subsequent triggers within 25 ns for detectors using TTS via TTC.

# **4.6 Software triggers**

The CTP will provide several different types of triggers in addition to physics triggers, i.e. those which are initiated by coincidences between different trigger inputs. The software triggers are initiated by a request from the CTP trigger processor. There are two types of software triggers. An asynchronous trigger is generated at the moment the trigger request is issued. A synchronous trigger is issued at a specific selected bunch crossing.

<sup>690</sup> During data taking detectors will require a number of different types of calibrations. These <sup>691</sup> can be fulfilled by generating a special class of triggers called calibration triggers. Cali-<sup>692</sup> bration triggers are treated as a special class of software triggers allowing the generation <sup>693</sup> of a calibration pulse before the readout triggers are sent [24].

For the upgrade in addition the heartbeat software trigger (see section 2.3.1) will be provided to designate the boundary between two data frames for continuous readout detectors and to provide a synchronisation check for local LHC counters.

<sup>697</sup> In order to perform these functions, three pieces of information need to be transmitted:

(a) a synchronous pulse marking the trigger, always at a fixed bunch crossing;

(b) 2 bits to mark whether the heartbeat trigger is normal or is also a start-of-data
 (SOD) or end-of-data (EOD) marker;

(c) 32 bits to transmit the orbit number.

	Unit cost	Number of units	Cost
	CHF		CHF
CTP	5000	4	20000
LTU	3000	30	90000
<b>Optical Splitter</b>	800	10	8000
Crate	10000	5	50000
Total			168000

Table 4.4: Cost Estimate.

On the TTC system, (a) and (b) are sent as a high priority short broadcast, while
 data (c) are sent as three long broadcast words of 12 bits. The format for the GBT
 protocol is more straightforward as the link offers a high data bandwidth.

# 705 **4.7 Funding and institutes**

The cost estimate for the trigger system consisting of CTP, LTU and optical splitters is given in Tab. 4.4.

<sup>708</sup> University of Birmingham take responsibility of the system design, implementation, pro-<sup>709</sup> duction and installation.

# **Chapter 5**

## 711

710

# **TPC/MCH readout ASIC - SAMPA**

Operating the TPC at a PbPb collision rate of 50 kHz requires the present limitations imposed by the operation of the gating grid to be overcome. Thus, the present MWPC based readout chambers will be replaced by GEM detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time will be higher than the average time between interactions a trigger-less, continuous readout is implemented. This implies the upgrade of the existing front-end ASICs to a new readout ASIC, the SAMPA ASIC, providing continuous readout.

Furthermore, in order to operate the muon chambers (MCH) with an interaction rate of 50 kHz the present front-end electronics cannot be used and will be replaced by the SAMPA ASIC. The SAMPA ASIC adapts to different detector signals with programmable parameters.

The SAMPA ASIC is an evolution of the presently used TPC front-end electronics, where 723 front-end amplifier and shapers sit in the 16-channel PASA ASIC [6][25]. The 16-channel 724 ALTRO [26] chip digitizes, processes, compresses and stores the data in a multi-event 725 memory. The Analog-to-Digital converters embedded in the chip have a 10-bit dynamic 726 range and are used in the TPC at 10 MHz. After digitisation, a pipelined Data Proces-727 sor is able to remove from the input signal a wide range of perturbations, related to the 728 non-ideal behaviour of the detector, temperature variation of the electronics and environ-729 mental noise. Moreover, the Data Processor is able to suppress the pulse tail within 1  $\mu$ s 730 after the peak with 1 % accuracy, in order to improve their identification. The signal is then 731 compressed by removing all data below a programmable threshold, except for a speci-732 fied number of pre- and post-samples around each peak. This produces non-zero data 733 packets. Eventually, each data packet is marked with its time stamp and size - so that the 734 original data can be reconstructed afterwards - and stored in the multi-event memory. A 735 further evolution of the system is the S-ALTRO ASIC [27]. The architecture is based on 736 the ALTRO ASIC. The main difference is the integration of the charge shaping amplifier 737 in the same IC. The SAMPA ASIC will integrate 32 channels of the full data processing 738 chain and support continuous and triggered readout. The design of the SAMPA has al-739 ready been started, taking the additional specifications compared to its predecessors into 740 account. 741



Figure 5.1: System block diagram



SAMPA contains positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal, that is digitized by a 10-bit 10 Msamples/s ADC. After the ADC a digital signal processor eliminates signal perturbations, distortion of the pulse shape, offset and signal variation due to temperature variations. SAMPA contains 32 channels per chip that concurrently digitize and process the input signals as shown in Fig. 5.1. The data readout takes place continuously at a speed of up to 1.28 Gbps by four 320 Mb/s e-links [11].

The data readout can be performed in continuous mode or triggered mode. In continu-750 ous mode the readout of a programmable number of samples is performed trigger-less 751 if the input signal exceeds the programmable threshold value. For the TPC application a 752 design rate of 50 kHz with 30 % occupancy is assumed. For the MCH the design rate 753 is 100 kHz and 10 % occupancy. Software triggers are acceptedreadout in continuous 754 mode for calibration and synchronisation purposes. In triggered mode data readout of 755 programmable number of samples is performed only upon reception of an external trig-756 ger with a maximum latency  $< 9.6 \ \mu$ s. Optionally all channels can be read out, not only 757 those crossing the threshold. Triggers arriving during an active readout will be accepted. 758 In that case the active readout will be extended by the new arriving trigger for the pro-759 grammable number of samples and status information is sent to acknowledge the readout 760 extension. Optionally a programmable number of pre/post samples before/after the input 761 signal crossed the threshold in continuous mode or the external trigger mode arrived can 762 be read out. 763

#### 5.2 ASIC building blocks



Figure 5.2: Block diagram of the SAMPA ASIC.

## 764 5.2 ASIC building blocks

The SAMPA ASIC is composed of a positive/negative polarity Charge Sensitive Amplifier 765 (CSA) with a capacitive feedback  $C_f$  and a resistive feedback  $R_f$  connected in parallel, 766 a Pole-Zero Cancellation (PZC) network, a high pass filter, two bridged-T second order 767 low pass filters, a non-inverting stage, a 10 Msamples/s 10-bit ADC and a Digital Sig-768 nal Processor(DSP) block, as shown in Fig. 5.2. Optionally the ADC can operate at 20 769 Msamples/s. The first shaper is a scaled-down version of the CSA and generates the first 770 two poles and one zero. A copy of the first shaper connected in unity gain configuration 771 is implemented in order to provide a differential mode input to the next stage. The sec-772 ond stage of the shaper is a fully differential second order bridged-T filter and it includes 773 a Common-Mode Feed-Back network (CMFB). The non-inverting stage adapts the DC 774 voltage level of the shaper output to use the full dynamic range of the ADC. It consists of 775 a parallel connection of two equally designed Miller compensated amplifiers. The ADC is 776 a differential 10-bit 10 Msamples/s SAR (successive approximation) ADC implemented 777 with a low power switching technique. The DSP part is composed of digital filters, a data 778 format unit, a ring buffer, a trigger manager block, a configuration register bank, a control 779 state machine, and four 320 Mb/s e-links. The chip will be fabricated in 0.13  $\mu$ m CMOS 780 technology. 781

Specification	TPC	MCH
Voltage supply	1.25V	1.25V
Polarity	Positive/Negative	Positive/Negative
Detector capacitance (Cd)	18.5pF	40pF - 80pF
Peaking time (ts)	80ns or 160ns	300ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 536e@ts=80ns*	< 950e @ Cd=40p*
	or < 482e@ts=160ns*	< 1600e @ Cd=80p*
Linear Range	100fC or 67fC	500fC
Sensitivity	20mV/fC or 30mV/fC	4mV/fC
Return to baseline time	<164ns@ts=80ns	<541ns
	or <288ns@ts=160ns	
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=80ns	< 0.2%@ts=300ns
	or < 0.2%@ts=160ns	
ADC effective input range	2Vpp	2Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10Msamples/s or 20Msamples/s	10Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
SFDR (ADC)**	68dBc	68dBc
SINAD (ADC)**	57dB	57dB
ENOB (ADC)	< 9.2-bit	< 9.2-bit
Power consumption (per channel)		
ADC	2mW (4mW)	2mW (4mW)
CSA + Shaper	6mW	6mW
Channels per chip	32	32

\* $R_{esd} = 70\Omega$ \*\* @ 0.5MHz, 10Msamples/s

Table 5.1: Specifications of the new front-end ASIC (SAMPA).

#### 5.2 ASIC building blocks

### 782 5.2.1 Front-end

Since the charge  $(Q_i)$  delivered by the TPC or MCH detectors is very small and short (typ-783 ically 7  $\mu$ A during 1 ns), it is unsuitable for immediate signal processing. Therefore, the 784 input signal is first integrated and amplified by the CSA producing at its output a voltage 785 signal ( $V_{CSA}$ ), whose amplitude is proportional to the total charge  $Q_i$  and characterized 786 by a long decay time constant  $\tau = R_f \cdot C_f$ . The  $C_f$  values are 600 fF@ts=80 ns , 1.2 787 pF@ts=160 ns and 2.4 pF@ts=300 ns, that are defined by the gain and linear range re-788 guirement and the  $R_f$  value of  $6M\Omega$  is defined by the noise specification [25][28]. The 789 relatively long discharge time constant of the CSA ( $\tau$ ) makes it vulnerable to pile-up. The 790 low frequency part of the pulse is then removed by the high pass filter  $(C_{dif} \cdot R_{dif})$ . Due 791 to the exponential decay of the CSA feedback network in combination with the differen-792 tiator network  $(R_{dif}, C_{dif})$ , an undershoot is created at the shaper output with the same 793 time constant as the CSA of  $\tau = R_f \cdot C_f$ . This undershoot is removed by creating a 794 pole-zero cancellation circuit by adding a resistance  $R_{pz}$  in parallel to the capacitor  $C_{dif}$ 795 in the differentiator stage. It creates a Zero in the transfer function that cancels the low 796 frequency pole introduced by the CSA feedback network [29][30]. The chosen topology 797 of the CSA amplifier (Fig. 5.3) is based on a single-ended folded cascode amplifier fol-798 lowed by a source follower. The CSA has been optimized for the specification of detector 799 capacitance and shaping time listed in Tab. 5.1. 800

The CSA shaping time can be configured to values of 80 ns and 160 ns for the TPC and 801 300 ns for the MCH. The sensitivity can be set to 20 or 30 mV/fC for the TPC and 4 802 mV/fC for the MCH by two external pins. As shown in Fig. 5.3a, switches  $S_1$ - $S_2$  are used 803 to adjust capacitances  $C_f$  and  $S_3$  -  $S_4$  to adjust  $C_{dif}$  for each case of peaking time. The 804 capacitors of the T-bridge network of the semi-Gaussian shaper are adjusted for 80 ns, 805 160 ns or 300 ns of shaping time achieved by placing additional capacitors in parallel. It 806 is performed with switches based on NMOS and PMOS transistors, sized to provide low 807 series resistance. The required sensitivity is controlled by  $R_G$  trimming (Fig. 5.2) which is 808 made by putting additional resistances in parallel. The maximum amplitude of the output 809 pulse is 2 Vpp. The output pulse waveform of the semi-Gaussian shaper is shown in 810 Fig. 5.3b for 160 ns of shaping time (20 mV/fC of sensitivity) and 300 ns of shaping time 811 (4 mV/fC of sensitivity). 812

The CMFB network of the second shaper stage establishes a stable common-mode voltage  $V_{CM}$  of 600 mV at the output of the second shaper. The chosen CMFB network consists of a resistor-capacitor network. This configuration takes the average of the two amplifier outputs and compares it with an externally given voltage  $V_{CM}$  and adjust the polarization current of the first stage of the amplifier.

A capacitive successive approximation (SAR) topology is used to design the 10Msamples/s 10-bit full differential ADC. The block diagram of the ADC is shown in Fig. 5.4. The main parts of the circuit are: capacitive array, switches, comparator and the SAR control logic. The capacitor array performs sample and hold and the digital to analog converter functions. A switching strategy with low energy dissipation per cycle is utilized.

The chip will be fabricated in TSMC 0.13  $\mu$ m CMOS technology with nominal voltage supply of 1.2 V. The analog blocks and digital blocks will have separate supply pads



Figure 5.3: (a) Transistor level schematic of the CSA; (b) Output pulse waveform of the semi-Gaussian shaper.

(Voltage supply and ground) with high isolation to avoid digital noise coupling. A 25  $\mu$ A stable current is generated on chip to bias the CSA and the Semi-Gaussian shaper (32 channels). An external resistor of high precision is used to control the bias current value. Another external resistance is used to control the bias of the ADC. It minimizes switching noise coupling from the ADC.



Figure 5.4: The block diagram of the 10b SAR ADC

### **5.2.2 Digital signal processing**

The signal processing is performed in 4 steps: a first correction and subtraction of the signal baseline, the cancellation of long-term components of the signal tail, a second baseline correction and zero suppression.

The first baseline correction (BC1) purpose is to decrease noise and systematic error effects. This block has two operation modes: subtraction mode and conversion mode. The subtraction mode consists of subtracting a value from the input ( $D_{in}$ ). This mode is divided in three kinds:

- Fixed: subtracts a constant value, called fixed pedestal, set previously in a register.
- Time dependent: subtracts a variable value which is stored in the pedestal memory (4096x10-bit). The values are accessed from first to last, so the order of the subtractions is the same for every processing window.
- Self-calibrated: a baseline value is calculated outside the processing window. It is called variable pedestal  $(V_{pd})$ , and its calculation is performed by an infinite impulse response (IIR) filter. If this option is selected, the filter is activated receiving as input  $D_{in}$  and providing  $D_{in} - V_{pd}$  as output, so  $V_{pd}$  is not accessible.

The conversion mode uses the input data to address the pedestal memory, so we have the output as a function of  $V_{in}$ .

The Tail Cancellation Filter (TCFU), is a 4-stage IIR filter used with the intention of cancelling a slowly varying signal. The signal rise time is fast, but its fall time is much slower and has a rather complex shape that varies from pad to pad.

The second level of baseline correction (BC2) is applied to the signal during the PTW (Processing Time Window) and corrects signal perturbations created by non-systematic effects. The threshold values have a constant component which is the same for the whole chip and a variable component which is channel specific so it must be set individually for each of the channels.

The zero suppression (ZSU) block eliminates data below a programmable threshold. An option to switch off the zero suppression is foreseen.

## **5.3 Configuration and control**

The SAMPA ASIC is configured via an independent serial interface. Data readout can take place at the same time. In order to keep compatibility with the GBT slow control adapter ASIC, SCA [17], SAMPA can be configured via an I2C interface. In addition, a high speed serial configuration and control interface operating at 320 Mb/s serial interface using one input and one output differential pair, is foreseen.

## **5.4 Trigger and dead time**

SAMPA supports two trigger modes: external and continuous mode. The readout works identically in both trigger modes. The number of samples per event is programmable (0 to 4095), as well as the number of pre-samples (0 to 63), which is the number of samples acquired before the external trigger arrived or the signal went above threshold. Also the number of post samples after the signal went below threshold is programmable (0 to 7). The number of samples per event and number of pre-samples are common to the 32 channels.

The trigger is sent either via an external pin or via an instruction with maximum latency  $<= 9.6 \ \mu s$ . In continuous mode the ASIC operates without an external trigger. It reads-out a channel when the data rises above a threshold in this channel and optionally reads-out the whole chip.

Provided the average interaction rate and occupancy does not exceed specifications the 876 SAMPA cannot get busy as it is specified for continuous readout. During operation the 877 interaction rate or occupancy might get too high for the design readout rate. In that case 878 the SAMPA data buffers will overflow. The SAMPA readout controller will truncate the 879 readout packets, balance the readout buffers and inform the DAQ in the data header that 880 truncation occurred. In triggered operation a trigger could be issued during an active 881 readout. In that case the reception of this trigger is acknowledged by sending a packet 882 trailer and the data readout is extended by the number of programmable samples. Pro-883 vided the interaction rate does not exceed specifications no data loss occurs. This feature 884 also allows accommodation of the periodic heartbeat trigger in both triggered mode and 885 continuous mode. After a heartbeat trigger the SAMPA needs to respond immediately 886 with a header/trailer and optional status information. Optionally the data readout before 887 the heartbeat trigger is continued or stopped. In any case there is no need to send a 888 fast busy signal to the TPC. Too many triggers are indicated in the trailers. Too much 889 data (too high occupancy or interaction rate) will fill the buffers and automatic truncation 890 is communicated to the DAQ. Under nominal operation conditions the SAMPA will not get 891 busy. However, in order to cope with unforeseen states where the SAMPA gets blocked, 892 the CRU forwards status information to the CTP which throttles or stops the triggers. This 893 transmission scheme is slower than a dedicated busy link from the front-end to the TPC 894 but completely sufficient for this purpose. 895

## 896 5.5 Readout

In continuous mode, once data are acquired they are formatted and stored in a FIFO, where they wait to be sent to the 320 Mb/s serial e-links, which send them off the chip. There are 32 channels and 4 e-links of 320 Mbit/s. Each e-link is connected to 8 channels transmitting either non-DC balanced or 8b10b encoded data stream. The readout controller polls the data FIFOs and reads them out in a round robin based fashion. The size of the data FIFOs still needs to be defined. It shall be done as a trade-off between chip area and probability of truncated events on high occupancy periods.

The TPC application defines the maximum data band width. It is designed for a channel occupancy of 30 % and a sampling rate of 10 MHz. Given the 32 channels \* a sampling rate of 10 MHz \* a word length of 10 bit \* 30 % occupancy, a data rate of 960 Mb/s per ASIC or 240 Mb/s per e-link needs to be accommodated. The 320 Mb/s e-links offer sufficient margin for transmission overhead. For pedestal runs, where the zero suppression is deactivated the readout is stopped when the buffers are full and restarted once they have been read out.

SAMPA operates with frame based readout. Once the readout starts, the header containing the bunch crossing counter, trigger origin and number of samples per event is sent. When the readout finishes a trailer containing the total number of 10-bit words on that event, data truncated and status information is sent. Also, a header-trailer pair is sent in order to tell the back-end electronics whenever the internal time stamping counter overflows and starts from zero.

When the SAMPA is operated together with the GBTx ASIC it receives a 40 MHz clock 917 from the GBT. This clock signal is used to align the SAMPA word boundaries to the trans-918 mission phase of the GBTx. In order to adapt the number of e-link outputs to application 919 data rate, the hit data can be routed through either all 4, 2 or 1 e-link, programmable via 920 instruction. Furthermore data from neighbouring ASICs can be routed to the ASIC output 921 (daisy chained readout) to further decrease number of output links in system. An addi-922 tional e-link input is available for this purpose. In the MCH application this allows daisy 923 chaining two SAMPA ASICs and the readout of one front-end card by one single e-link 924 only. For test purposes of the detector system and the online computing system SAMPA 925 allows to send pre-programmable data sequences. The SAMPA data flow block diagram 926 is shown in Fig. 5.5. 927

### 928 5.6 ASIC I/Os

All the digital IO of the SAMPA ASIC are differential SLVS ports. The following list describes the SAMPA periphery:

- 931 Digital inputs:
- Digital clock: 320 MHz, a jitter of less than 30 ps RMS is expected.



Figure 5.5: Data block diagram

- ADC reference clock: 10 MHz, optionally it can be produced from the digital clock. The phase of the ADC reference clock can be adapted to the GBT alignment clock.
- GBT alignment clock: 40 MHz, this signal allows alignment to the GBT transmission word phase.
- Reset global: resets all registers.
- Sync: This signal resets internal event counter and time stamp.
- Trigger: external trigger signal, synchronised to internal 40 MHz with programmable phase.
- e-link data input: allows merging data stream of neighboring ASIC.
- Address: 5 bit hard-coded address field which can be read via the configuration ports.
- High speed serial instruction input (8b10).
- Sensitivity control (gc0 and gc1): 2 pin (This value also can be programmed)
- Shaping time control (ptc0 and ptc1): 2 pin (This value also can be programmed)
- 947 Digital outputs:
- 4 e-link outputs: 320 Mbit/s data stream, programmable non-DC balanced or 8b10.
- Readout active signal:
- Full signal: is active, when buffers in the ASIC are full, data loss occurs and data readout is truncated.
- High speed serial instruction output (8b10).
- 953 Digital Input/Outputs:
- I2C interface.

ptc0	ptc1	gc0	gc1	Shaping time	Sensitivity
0	0	0	0	160ns	30mV/fC
0	0	1	0	160ns	20mV/fC
0	0	0	0	80ns	30mV/fC
0	0	1	1	80ns	20mV/fC
1	1	1	1	300ns	4mV/fC

Table 5.2: Gain an shaping time programming options of the ASIC.

955 Analog inputs:

- 32 Detector inputs: 32 pins
- External bias resistances: 2 pins
- Reference voltages ( $V_{REF-}$ ,  $V_{REF+}$ ): 2 pins
- Common voltage  $(V_{CM})$ : 1 pin

<sup>960</sup> The sensitivity and shaping time programming options of the ASIC are listed in Tab. 5.2.

# **5.7** Schedule, funding and institutes

The project schedule is presented in Fig. 5.6. Presently the project is in the design phase.
 The analog blocks are ready to start the layout phase.

<sup>964</sup> Two prototyping runs (MPW: Multi-Project Wafer) will be performed:

 The first run planned for November of 2013 will contain each block separately and a complete version of one channel (Preamplifier, Shaper, ADC and digital blocks). The test boards will be designed and implemented by Polytechnic School of the University of Sao Paulo or by the ALICE collaboration. The radiation tolerance test will be performance at Nuclear Physics Department of USP. More detailed tests will be conducted by the TPC and MCH Team.

- 2. The second run is planned for August 2014, which will contain the 32 channels, all integrated on one die. The purpose is to test the whole system, among them: power consumption, the noise and crosstalk performance.
- <sup>974</sup> The final chip is being planned to be produced in May of 2015.

In Tab. 5.3 SAMPA cost estimate is made. The estimate assumes prices for a similar technology, as TSMC prices available via the CERN frame contract are not yet available.
The cost estimate is based on 2 multi project engineering runs (MPW), 2 full scale submissions, a final ASIC size of 65 mm<sup>2</sup> and an ASIC yield of 60 %. Using these numbers this estimate refers to a upper price limit. On one wafer a silicon area of 25200 mm<sup>2</sup> (60



Figure 5.6: Schedule of the TPC/MCH readout ASIC project

reticles x 21 mm x 20 mm) is assumed, corresponding to 387 ASICs per wafer and, ap plying the yield, 232 working ASICs per wafer. In total 52000 ASICs are needed (without
 spares) and thus 224 wafers or 250 wafers with spares included are required. Assuming
 3500 USD per wafer the production cost is 875 kUSD.

<sup>984</sup> The project has the following funding sources:

- 1. Special program for integrated circuits fabrication of Brazilian Public Universities.
- 2. Regular project submitted in February 2013 to FAPESP with:
- MPW (US\$ 145K)
- Test board fabrication
- Scholarships
- Two Trips to CERN
- Publications
- 3. FAPESP project will be submitted for the Engineering Fabrication Run

993 Production funding options:

### 5.7 Schedule, funding and institutes

item	cost
MPW	2 * 50 kUSD
Full scale submission	2 * 400 kUSD
Wafer production	875 kUSD
Total	1775 kUSD
Number of MCH + TPC SAMPA	52000
Price per ASIC out of 52000	34 USD
Packaging & testing per ASIC	10 USD
Price per packaged and tested ASIC incl. 10 % spares	44 USD
Price per packaged and tested ASIC incl. 10 % spares	40 CHF

Table 5.3: SAMPA cost estimate.

- FAPESP agency: Sao Paulo research foundation (state level).
- Ministry of Science, Technology and Innovation (federal level).
- University of Sao Paulo.
- CNPq agency: National Counsel of Technological and Scientific Development (federal level).
- <sup>999</sup> Table 5.4 shows the involved institutes.

#### Institutes

EPUSP, Escola Politécnica, Universitade de São Paulo, Brazil IFUSP, Instituto de Fisica, Universidade de São Paulo, Brazil University of Bergen, Norway IPNO, Institut de Physique Nuclaire d'Orsay, Université de Paris-Sud, IN2P3/CNRS, France SPhN, Service de Physique Nuclaire, CEA-IRFU Saclay, France

Table 5.4: SAMPA institutes.

1000

1001

# **Chapter 6**

# Muon tracking CHambers - MCH

### 1002 6.1 Introduction

The muon chambers (MCH) consist of 156 multi-wire proportional chambers with more than one million electronics channels. In order to support the interaction rate of 50 kHz, the design readout rate has been set to 100 kHz as safety margin. Approximately 34000 front-end ASICs and 17000 front-end cards need to be replaced and are connected via  $\approx$  500 GBT optical links to the common readout (CRU). The front-end readout uses the SAMPA ASIC, which supports triggered and continuous readout.

### **6.2 The present system**

The muon chambers are based on multi-wire proportional chambers with cathode pad 1010 readout, the so called Cathode Pad Chambers. The system consists of 5 tracking sta-1011 tions, each station composed of 2 chambers. Because of the different sizes of the sta-1012 tions, (ranging from few square metres for station 1 to more than 30 m<sup>2</sup> for station 5) two 1013 different designs were adopted. The first two stations are based on a quadrant structure 1014 [31], with the readout electronics distributed on their surface (see Fig. 6.1 (Left)). Four in-1015 dependent quadrants constitute one chamber. For the bigger stations, a slat architecture 1016 [32] was chosen (see Fig. 6.1 (Right)). The maximum active size of a slat is  $40 \times 240$ 1017 cm<sup>2</sup> and the electronics is implemented on the top and bottom part of each slat. Slats are 1018 mounted on a frame support to constitute one half-chamber. One half-chamber consists 1019 of 9 slats for station 3, and 13 slats for station 4 and 5. The total number of detectors is 1020 156, 140 slats and 16 quadrants. The slats and also the quadrants overlap to avoid dead 1021 zones on the detector. The tracking system covers a total area of about 100 m<sup>2</sup>. 1022

<sup>1023</sup> The present electronics contains the front-end electronics and the readout system, CRO-<sup>1024</sup> CUS (Cluster Read Out Concentrator Unit System), which concentrates the data signals from the front-end electronics (FEE) and sends them to the Data Acquisition System (DAQ) on optical fibers and to the interface with the ALICE Central Trigger Processor. Data, control and trigger signals are transmitted on buses burried in the detector PCBs and on ribbon cables between the detector and the CROCUS. Translator boards located on the external edges of the detectors make the link between buses and ribbon cables to adapt the signal levels and allow an easy connection/disconnection of the detectors.

# **6.3 Muon system upgrade**

In order to achieve a design readout rate of 100 kHz an architecture has been adopted
 where the signals are continuously sampled. The dead time free data readout supports
 a continuous, self-triggered readout mode and triggered mode. The data flow will be
 reduced by the online computing system and then sent to the offline system.

The muon chamber electronics upgrade architecture employs ALICE common electronics developments, the front-end ASIC, SAMPA used by MCH and TPC (see chapter 5) and the common readout unit (CRU). Programmable parameters in the SAMPA allow to take specification differences between the two systems into account. The Common Readout Unit (CRU) will replace the CROCUS boards to concentrate the data before transmitting them to the DAQ. The data transmission between FEE and CRU is based on optical GBT links.

### 1043 6.3.1 Front-end electronics

- <sup>1044</sup> The FEE parameters are defined by the following specifications:
- The detector implementation will not be modified. Therefore the location, physical layout and connections to the chambers of the 64 channel FEE boards will be unchanged.





Figure 6.1: Left: Layout of station 2 of the muon chambers; the readout electronics is distributed on the surface of a quadrant. Right: Layout of stations 4 and 5 of the muon chamber system; the readout electronics is distributed on the top and bottom edge of the slats.

### 6.3 Muon system upgrade

- The chambers will be operated with the present gas and HV parameters (gain:~ 2·10<sup>4</sup>, good charge spread).
  The spatial resolution is better than 100 μm, which corresponds to a required charge resolution at the percent level.
  The maximum input signal will be 500 fC and the gain ~ 4 mV/fC, considering an 2 V effective ADC range.
- The cooling system remains unchanged allowing no significant increase in power consumption ( $\simeq$  13 mW/ch).

For the expected signal distribution, the dependence of the charge and spatial resolution 1056 on shaping time, sampling frequency, ADC resolution and noise has been studied. Shap-1057 ing times of 160 ns, as for the TPC application and 300 ns, have been considered. Three 1058 sampling frequencies, 10, 25 and 40 MHz and three different ADC resolutions with 10, 11 1059 and 12 bit respectively have been evaluated [33]. In order to avoid resolution degradation 1060 due to the suppression of ADC samples before/after each trigger, when the signal has 1061 not yet/already exceeded/crossed the threshold, the SAMPA ASICs allow transmission of 1062 a programmable number of pre and post trigger samples. 1063

- <sup>1064</sup> The parameters for the MCH have been found to be as follows:
- 10 bit ADC resolution,
- 10 MHz sampling rate,
- shaping time of 330 ns,
- noise below 2000 electrons (large pads), 1000 electrons (small pads).

1069 .

### 1070 6.3.2 Readout electronics

<sup>1071</sup> The muon chambers have 17000 FEE boards with two 32-channel SAMPA ASICs each <sup>1072</sup> connected to GBT readout boards. Physically two different types of FEE cards are used <sup>1073</sup> for the quadrants and the slats. This configuration is illustrated in Fig. 6.2.

The SAMPA output data rate is sufficiently low that the data traffic is routed through only one single SAMPA e-link [34] operating at 80 Mbit/s. One of the two SAMPA readout ASICs on the FEE card sends its data readout stream to the other SAMPA on the FEE card. This SAMPA multiplexes the data stream of its neighbour with its own data stream. That way each FEE card has only one single e-link as output.

<sup>1079</sup> The data transmission from the FEE cards to the CRU in the counting room is done <sup>1080</sup> via bi-directional GBT links. Each FEE e-link is connected to one out of 40 GBT e-<sup>1081</sup> link inputs. These e-links carry the detector data and trigger/timing information. The maximum distance is 2.5 m which is a comfortable distance for the 80 Mbit/s e-links. The
 GBT link chip set is a common LHC development and contains the GBTx ASIC, SCA
 ASIC and the optical transceiver module VTRx [35]. The GBTx transmits detector data
 and receives timing and trigger data via the VTRx optical transceiver. The slow control
 adapter ASIC (SCA) is directly connected to the GBTx and allows communication via I2C
 to the SAMPA ASICs and allows the measurement of supply voltages.

As the trigger latency for the MCH is not critical, the CTP sends trigger and timing information via the trigger and timing distribution system (TDS) to the counting room. There it is distributed to the CRU and forwarded to the FEE cards via the bi-directional GBT links. The CRUs are connected to the DAQ via the DDL3 interfaces, send the detector data to the first level processors (FLP) and receive DCS information via the FLPs from the ALICE DCS which is merged with the trigger information into the GBT link. In total 500 GBT based transceiver cards and links are required.

The muon chamber electronics will support readout upon a trigger signal at interaction rate as well as a trigger-less, continuous readout designed for an maximum interaction rate of 100 kHz. The external trigger signals include the interaction trigger, software trigger for pedestal and calibration (100 Hz) and commission triggers.

### 1099 6.3.3 Data rate and format

In addition to the raw data output of the acquired ADC samples, the MCH applies a
 compression directly performed by the SAMPA where the charge and a time stamp is
 read out only. A simple sum of sampling values including a programmable number of pre and post samples is foreseen. Nominally 1 pre-sample and 1 post sample is considered.

For data bandwidth considerations, an occupancy of 9% and an interaction rate of 100 1104 kHz is assumed. The considerations for the data word length assume a maximum pulse 1105 width over threshold with 330 ns shaping time of 1000 ns corresponding to 10 samples 1106 over threshold at 10 MHz sampling rate. 64 bit data words have been considered for 1107 one channel in the charge output mode, whereas 140 bit for the raw mode are assumed 1108 (header/trailer with time stamp and channel address: (20 bit) + 10 + 1 pre + 1 post ADC1109 samples (120 bit)). The system needs to be designed for the higher data rate of these 1110 two modes. As a result each FEE channel e-link carries in average a data amount of pprox1111 80 Mb/s considering 9 % occupancy \* 100 kHz interaction rate \* 140 bit word length \* 1112 64 channels. It should be noted that the application of 100 kHz readout rate compared 1113 to the 50 kHz interaction rate already implies a factor 2 safety. In total the MCH system 1114 is designed for a maximum data rate of 1600 Gb/s (9 % occupancy, raw data sample 1115 readout, 100 kHz trigger rate). 1116

# 1117 6.4 Schedule, funding and institutes

<sup>1118</sup> The cost estimation of the muon chamber electronics upgrade is given in Tab. 6.1.

60



Figure 6.2: MCH readout configuration.

The involved institutes are are shown in table 6.2. For the common developments (CRU & SAMPA) cost sharing with the involved institutes is anticipated. The FEE boards and GBT boards will be taken in charge, both technically and financially, by the muon laboratories: Orsay (IN2P3) will design and produce the FEE boards. Cagliari (INFN) and IRFU (CEA Saclay) will design and build the links/cables and GBT boards.

Common parts will be taken in charge partly by muon laboratories and the involved laboratories: Budapest and India groups are responsible for the CRU design and production; the financing will involve these two groups but also the muon chamber laboratories. The design and the production of the FEE chip, SAMPA, is coordinated by the Brazilian team, which will be the main contributor; IRFU is involved in the FEE chip design.

Table 6.3 shows the schedule for upgrade development items.

Item	#	Price	Total cost
		[CHF]	[kCHF]
SAMPA	38000	37	1406
FEE board	19000	32	608
(PCB+passive comp.)			
FE2GBT cable	19000	15	285
FE2GBT card	500	200	100
(PCB+passive comp.)			
VTRx	500	200	100
GBTx	500	60	30
SCA	500	10	5
FE-link (passive)	500	300	150
CRU (# of inputs)	500	316	158
trigger distribution	1	10	10
Total			2852

 Table 6.1: Cost estimation for the muon chamber electronics upgrade, including 10 % of spare (CORE cost only)

In	oti.	<b>t</b> i i'	tne
	511	ш	105

INFN and Università degli Studi di Cagliari, Italy IPNO, Institut de Physique Nuclaire d'Orsay, Université de Paris-Sud, IN2P3/CNRS, France SPhN, Service de Physique Nuclaire, CEA-IRFU Saclay, France UNICAMP, Universidade Estadual de Campinas, Brazil IFUSP, Instituto de Fisica, Universidade de São Paulo, Brazil EPUSP, Escola Politécnica, Universitade de São Paulo, Brazil Wigner Research Centre for Physics, Institute for Particle Nuclear Physics, Hungary VECC, Variable Energy Cyclotron Center, Department of Atomic Energy, Kolkata, India SAHA Institute of Nuclear Physics, Kolkata, India

Table 6.2: MCH institutes.

Item	
FEE board	2014
FE2GBT cable	2014
FE2GBT card	2014
system test	2016
system installation	2017

Table 6.3: MCH Time schedule.

1130

1131

# Chapter 7

# **Muon Identifier - MID**

### 1132 **7.1 Overview**

The Muon Identifier (MID) is the proposed future designation, after LS2, of the present 1133 Muon Trigger system [2]. This choice will be justified in what follows. It is briefly recalled 1134 that the Muon Trigger detector is composed of 4 planes of single gap Resistive Plate 1135 Chamber (RPC) detectors, organized in two stations of two planes located at 16 m and 1136 17 m from the interaction point. The planes in the same station are 17 cm apart. The 1137 total detection area is about 150 m<sup>2</sup>. The RPC signals are collected by means of a total 1138 of 21000 strips and the same number of Very Front-End (VFE) electronics channels. 1139 The signals from the VFE electronics are propagated to the Front-End (FE, essentially in 1140 charge of taking the muon trigger decision) and readout electronics. 1141

The VFE electronics is located on the RPC detectors and its upgrade has been already discussed in the Letter of Intent (LoI) for the ALICE upgrade [1]. The main motivation is to prevent ageing of the RPCs. The present VFE chip called ADULT [36] will be replaced by a new ASIC, FEERIC. Unlike ADULT, FEERIC will perform amplification of the analog signals from the RPCs. The RPCs will be operated in "genuine" avalanche mode (like in ATLAS [37] and CMS [38]) with a significant reduction of the charge produced in the gas, hence limiting ageing effects.

In the Lol, it was proposed to preserve the muon trigger decision functionalities and to
read out the muon spectrometer upon a muon trigger with a rate that is typically one order
of magnitude smaller than the PbPb minimum bias interaction rate. Specifically, it was
proposed to keep the FE (so-called local) cards and only upgrade the readout electronics.
The local cards presently receive the signals from the VFE and deliver the first stage of
the muon trigger decision. It was however identified that the future L0 trigger latency
requirement might be difficult to fulfil.

Subsequently to the LoI, it has been decided to change this strategy and read out the muon spectrometer for each minimum bias trigger with the goal of maximizing its physics potential. This implies some changes in the upgrade strategy because :

200 kHz pp $\sqrt{s}$ = 14 TeV	100 kHz PbPb $\sqrt{s}_{NN}$ = 5.5 TeV
6 (mean) - 15 (peak) hits/s/cm <sup>2</sup>	75 (mean) - 125 (peak) hits/s/cm <sup>2</sup>

Table 7.1: Expected counting rates of the RPCs.

- the readout rate will be more than one order of magnitude larger compared to the initial design;
- there is no need for fast, hardware based,  $p_T$  dependent muon trigger signals.

As a consequence the entire FE and readout electronics must be replaced in order to 1162 cope with the given readout rates. Since the muon trigger functionalities are abandoned, 1163 a simplified design can be implemented. The detector, separated from the Muon Tracking 1164 system by an iron wall of 1.2 m thickness, will however keep its crucial role as muon iden-1165 tifier which motivates the change of name to MID. Indeed, the hadron contamination in the 1166 Muon Spectrometer, for matched tracks with the ones in the MID, is dramatically cleaned 1167 [39, 40] and all present data analyses request this matching condition. Finally, the MID 1168 should help to reduce pile-up effects in the Muon Spectrometer when track matching is 1169 requested thanks to its excellent timing properties allowing the separation of two tracks 1170 belonging to two adjacent 40 MHz bunch crossing cycles. 1171

- <sup>1172</sup> In conclusion the upgrades MID system during LS2 consists in:
- Replacement of the VFE electronics;
- Replacement of all FE and readout electronics.

<sup>1175</sup> There is no indication for a need of a major upgrade of the RPC detectors and gas system <sup>1176</sup> and only some maintenance operations are expected.

# 1177 7.2 Very Front-End electronics upgrade

The expected counting rates of the RPC detectors are given in Tab. 7.1 for pp and PbPb. These values are extrapolated from the present measurements [41]. The counting rate in pp does not account for the beam induced background which can be quite large.

It can be seen from Tab. 7.1 that the counting rate of the RPC could exceed 100 hits/s/cm<sup>2</sup> 1181 in PbPb collisions. As discussed in [1], in the current operating mode of the RPCs, without 1182 amplification in the VFE, the mean total charge is of the order of 100 pC per hit. In these 1183 conditions the R&D results [42] on efficiency set an instantaneous counting rate limit 1184 below 50 hits/s/cm<sup>2</sup>, including some safety margins in case of short running periods. An-1185 other limitation comes from RPC aging : from our R&D [42], safe operation of the detec-1186 tors cannot be guaranteed for a cumulated dose larger than 50 mC/cm<sup>2</sup> (500 Mhits/cm<sup>2</sup> 1187 in the present mode of operation). 1188

The total particle fluence numbers for the upgrade physics program and safety factors discussed in Chap. 3 would result in a charge deposit of more than 100 mC/cm<sup>2</sup> for the

64

### 7.2 Very Front-End electronics upgrade

most exposed RPCs. Keeping in mind that the RPCs will have accumulated already an significant dose before LS2, these arguments strongly favour operating the RPCs in "genuine avalanche" mode, with a reduced charge per hit. Based on e.g. ATLAS results [43], a reduction by a factor 3-5 for the charge per hit can be achieved, which requires the mentioned change of the VFE electronics.

<sup>1196</sup> A R&D program has been launched in order to evaluate the actual performance of the <sup>1197</sup> MID RPCs equipped with the new VFE electronics and is described as follows:

- measurement of the channel noise for the RPC installed in the cavern, which gave values in the range of 25 - 50 fC depending on strip size and position.
- realization of a VFE card prototype called BARI-FE (Fig. 7.1) with the CMS RPCs ASIC[44];
- measurements of the RPC performance (efficiency curves, time resolution, cluster size) with BARI-FE prototypes on the Torino RPC production test bench [45];
- design of the FERRIC ASIC.



Figure 7.1: VFE card with the first prototype of the FEERIC ASIC.

The efficiency curves for RPCs equipped with BARI-FE cards (for threshold values of 200 mV and 250 mV) and ADULT cards (with 7 mV threshold without signal amplification) are compared in Fig. 7.2.

As expected, It can be seen that the voltage at the efficiency knee is shifted towards 1208 lower values, by several hundreds of volts with BARI-FE. As a direct consequence, the 1209 charge at operating voltage is lower. From test bench measurements, it is difficult to 1210 evaluate the charge per hit achievable in cavern at operating voltage which depends in 1211 turns on the threshold value hence on the noise level. For this reason we foresee to 1212 equip before the end of the LS1 one of the ALICE RPC in cavern with a FEERIC VFE 1213 card pre-production (typically 50 cards of 8 channels each) in order to quantify accurately, 1214 on a long time scale, the achievable RPC performance in realistic conditions. The VFE 1215 production would follow, for a final installation scheduled during the LS2. The possibility 1216 of using the I2C bus for threshold remote control is considered. 1217

As there is no available ASIC fulfilling all MID requirements the design of the FEERIC ASIC has been carried out. The CMS RPC ASIC is the closest to the needs but it is designed for negative signals only while the MID is readout on both sides of the RPC



Figure 7.2: Comparison of efficiency curves for RPCs equipped with the BARI-FE and ADULT VFE cards

plane and thus requires positive and negative signal processing. The block diagram of the FEERIC is shown in Fig. 7.3. It includes a two stage transimpedance amplifier with  $\approx 0.1 \Omega$  input impedance, a zero-crossing discriminator, a one-shot preventing from retriggering during 100 ns and LVDS drivers.



Figure 7.3: Block diagram of the FEERIC ASIC

The main specifications, requirements and simulated performance of the FEERIC ASIC are summarized in Tab. 7.2. The operating range is expected to be above a threshold of typically 100 fC.

The first prototype of the FEERIC ASIC has been delivered at LPC Clermont-Ferrand in September 2013. Qualification tests are ongoing : preliminary measurements (Tab. 7.2) show that this first version of the ASIC is fully operational. A second submission will be launched by early 2014 to optimize the ASIC performance while fine tuning its layout. The FEERIC VFE card pre-production will be built using the ASIC from this submission.

### 7.3 Front-end and readout electronics upgrade

	FEERIC ASIC	FEERIC VFE card
	specs, reas and	prototype performance
	simulated performance	
ASIC technology	0.35 μm CMOS	X
Number of ch.	8	Х
Dynamic range	Q=20 fC - 3 pC	Х
Noise level	< 2 fC (r.m.s.)	25 fC (noise limit)
Power cons.	70 mW/ch	60 mW/ch
	Req. <100 mW/ch	
Power supply	3 V	Х
Input polarity	+/-	Х
Amplification	0.4 mV/fC	0.33 mV/fC
One shot	yes (100 ns)	Х
Discriminator	zero crossing	Х
Time resolution r.m.s.	< 200 ps	< 500 ps
for $Q > 100 fC$	Req. <1 ns	
Time walk	600 ps	900 ps
for $100 < Q < 3000 \text{ fC}$	Req. < 2 ns	
Output signal format	LVDS, 23 $\pm$ 2 ns	Х

 Table 7.2: Main specifications, requirements and simulated performance (central column) of the FEERIC ASIC; Measured performance (right column, preliminary) of the first prototype of the FEERIC VFE card

## 7.3 Front-end and readout electronics upgrade

The present MID is divided into 16 vertical regions. Each of the 16 regional areas is read out by 1 out of 16 VME crates. Each crate contains one regional card multiplexing the data from up to 16 local cards. Each local card is connected to 128 VFE channels via eight cables with each 34 wires from four detector planes and the two orthogonal coordinates. In total 234 local cards are used. The system is located on the upper gangways at the C-side where the radiation level is low. For the upgrade this segmentation will be maintained.

Figure 7.4 shows the upgraded MID system architecture. In order to increase the readout rate to 100 kHz both the local and regional readout cards well be re-designed. The hardware implementation of the regional and local card will be identical, reducing the design and production effort by re-using the same hardware and adapting the FPGA firmware.

The local card receives the binary chamber signals via LVDS signals indicating whether the corresponding channel has been hit for each bunch crossing. The FPGA in the local card performs the following functions:

- it applies a remotely configurable noisy channel mask;
- compensates the different transmission delays (max.: 35 ns, per steps of 2.5 ns) from cables of different lengths coming from the VFE;



Figure 7.4: FE and readout electronics architecture

Component	Number
VFE cards/channels	2384/20992
Local cards	234
Regional cards	16
CRU AMC cards	1
e-links	234
GBT (bi-directional)	16
DDL3	1

Table 7.3: Total number of MID cards and links

- calculates a Loc-trk signal for each bunch crossing corresponding to a track crossing in any of the two detector stations;
- provides 16-bit counters for monitoring the detector counting rate;
- zero-suppresses the input data;
- provides a multi-event buffer;

• and provides a trigger, clock, control and data interface to the regional card using one 320 Mbit/s serial bi-directional connection;

The same card, used as regional card receives the local information via 16 serial links, 1259 assembles the raw events in their final format, adds the trigger information. The cards 1260 offer two bi-directional 3.2 Gbit/s GBT links to send the data to the CRU in the counting 1261 room, which forwards the MID data on one DDL3 link to the DAQ FLPs. For the data 1262 rate in the MID one GBT link per regional card is sufficient. However, it is foreseen to im-1263 plement a second link on the regional card for redundancy and possible further upgrade. 1264 The regional card provides a Reg-trk signal for each bunch crossing  $\approx$  300 ns after the 1265 interaction by ORing the local Loc-trk signals. Fig. 7.5 shows a block diagram of the lo-1266 cal/regional hardware implementation. The number of cards and links is summarized in 1267 Tab. 7.3. 1268

As the MID in not latency critical the trigger and timing interface (TTS) based on GBT links

connects the MID via the LTUs and the CRU in the counting room. From there the CRU
 forwards the trigger and timing information via the GBT front-end links to the regional and
 local cards.

<sup>1273</sup> The adopted architecture, has the advantage of limiting the number of high speed GBT <sup>1274</sup> links thanks to the regional interface between the local cards and the CRU. The cost of <sup>1275</sup> the project is consequently reduced.



Figure 7.5: New local/regional card scheme: the specific local (regional) components are represented in cyan (magenta) while the common ones are in black

Events are stored in the local card multi-event buffer at each trigger. The range of the acceptable trigger latency is 0.5-9.6  $\mu$ s. The multi-event buffer in the local card is larger than the size of one software event (registered at very low rate) which includes, in addition to the standard physics event information, the counters. The maximum size of a software event, obtained in case of calibration events with the front-end test (FET) generator for which zero suppression is not efficient, because all strips are fired, is 50 words of 32 bits. It corresponds to a depth of 10 physics events (maximum 5 words of 32 bits).

The implementation of 2 GBTs per local/regional card leaves the option of a complete VFE data transfer (5.12 Gbit/s), at 40 MHz without zero suppression, from the local cards directly to the CRUs (typically one CRU per regional area in this case). This solution corresponds to a continuous readout, however, with an increased cost due to the higher number of optical GBT links to the CRUs.

The expected data flow in pp and PbPb is given in Tab. 7.4. It includes a preliminary evaluation of event separators and headers which contribute significantly to the event size. The total data flow in PbPb at 100 kHz amounts to 300 MB/s. The readout dead time is expected to be negligible with a single DDL3 link at 10 Gbit/s. Anyhow a busy mechanism will be implemented.

200 kHz pp $\sqrt{s}$ = 14 TeV	100 kHz PbPb $\sqrt{s}_{NN}$ = $5.5~{ m TeV}$	
Total data flow	Total data flow	Max data flow per link
to DAQ	to DAQ	from local to regional card
540 MB/s	300 MB/s	1 MB/s

Table 7.4: Expected data flow

	R&D, Pre-prod	prod		instal	
	2014	2015	2016	LS2	Total
VFE + RPC	40	200	120		360
FE + Readout	40	130	130		300
Total	80	330	250		660

Table 7.5: Schedule and funding in kCHF (CORE cost only)

# 7.4 Schedule, funding and institutes

1294 The involved institutes are :

- Sezione INFN and Dipartimento dell'Università di Torino, Italy
- Konkuk University, Seoul, Republic of Korea
- Subatech, Ecole des Mines et Université de Nantes, France IN2P3/CNRS
- Laboratoire de Physique Corpusculaire, Université Blaise Pascal de Clermont-Ferrand,
   France IN2P3/CNRS

Table 7.5 shows funding and schedule with a start of local/regional card prototyping during LS1, CRU interfacing and local/regional card production in 2015 - 2016 and installation and commissioning during LS2.

# **Chapter 8**

# Transition Radiation Detector - TRD

### **1305 8.1 TRD upgrade strategy**

1303

The Transition Radiation Detector (TRD) has originally been designed for a *Pb-Pb* interaction rate of 8 kHz and for a significant event rejection from the level 1 (L1) trigger [46]. The existing processing and readout of the front-end electronics (FEE) as well as the readout and trigger functionality are optimized for these conditions and to provide a fast L1 trigger contribution, implementing jet and electron triggers.

For the ALICE upgrade, the TRD detector must operate at much higher interaction rates, and the FEE and readout system must accept the largest possible fraction of interactions without the need to provide a trigger.

Based on measurements in Pb-Pb collisions in Run 1, it has been estimated that the 1314 chamber currents reach 6  $\mu$ A at 50 kHz interaction rate. This leads to a total accumulated 1315 charge of 0.8 mC per cm of wire per year, assuming an average interaction rate of 50 kHz. 1316 As the chambers were validated for charges above 10 mC/cm, it is expected that no 1317 ageing effect will occur for the planned running time. The voltage drop at these currents 1318 however may result in significant gain variations in case of large variations of interaction 1319 rate, e.g. over the duration of a fill. No problems on detector stability or concerning space 1320 charge effects are expected. 1321

An upgrade of the FEE hardware is not realistically feasible. Besides the design and production effort, it would require a complete disassembly and rebuild of the 18 TRD supermodules and the FEE mounted on the 522 individual detector chambers. The chosen strategy is a reduction of event readout time with the existing FEE by changing its mode of operation and limiting the amount of event data read from the FEE as detailed in Sec. 8.2. The impact on performance for tracking and electron identification has been extensively studied (see Sec. 8.3) to validate the proposed strategy. The readout of the optimized FEE data format at the full minimum bias event rate requires new hardware with increased bandwidth to the DAQ system as described in Sec. 8.4. The use of the proposed ALICE Common Read-Out Unit is envisaged for this purpose.

# **8.2 Frontend operation and readout**

### 1333 8.2.1 Current FEE readout

In contrast to the continuous readout strategy of other ALICE detectors, the TRD FEE [47] is bound to operate in a triggered mode of single event readout. An initial trigger level (LM - Level Minus one; the functionality corresponds to the "pretrigger" in Run 1) fixes the time reference for sampling and processing. A subsequent event can only be triggered on after completion of the FEE event readout or of the abort sequence after a negative higher level trigger.

The front-end electronics comprises a hardware preprocessor for the calculation of quantities relevant for the finding of online tracklets, which are track segments in a single detector chamber. The preprocessor provides its results at a fixed time after the sampling has been started by a LM trigger. Further processing is done in CPUs in the FEE.

Fig. 8.1 shows the timing sequence for a typical event. To recover the information before the arrival of the LM trigger, the digitized data are delayed in pipeline stages. With a drift time of 2.2  $\mu$ s and a delay of 900 ns the processing in the CPUs can start 3.1  $\mu$ s after the interaction when all data have passed through the preprocessor and its results are available. The processing time depends on the complexity of the calculations, finding tracklets using the preprocessor results takes about 1  $\mu$ s.

The FEE readout is organized in 60 trees (2 per chamber) per supermodule, each with 64 1350 FEE devices (multi chip module - MCM) and equipped with one optical readout interface 1351 (ORI). The readout can operate in two modes, tracklet mode and raw readout mode. The 1352 tracklet mode is implemented as pure push mechanism up the readout tree without any 1353 handshaking. This avoids latency but is limited to the readout of 4 32-bit words for each 1354 MCM. The raw readout mode has no practical limitation on the number of transmitted 1355 words but requires handshaking, which results in a total overhead of 8.32  $\mu$ s per readout 1356 tree in addition to the time for the actual data transfer with 8 bit at 120 MHz. 1357



Figure 8.1: FEE event processing and readout sequence as used in Run 1. The event readout timing is shown for an event with 25% of tracklet words.
### 8.2 Frontend operation and readout

The event readout time, i.e. the time from an interaction until the FEE has finished shipping all data, depends on the FEE processing effort and the maximal data volume in a single readout tree. With the raw readout mode, the event readout time will be of about 16  $\mu$ s in addition to the transfer time for the actual data volume of a given event. The currently used readout of full zero-suppressed ADC data results in event readout times of several 10  $\mu$ s and puts a severe limit on the maximum readout rate.

### **8.2.2 Readout with modified data formats**

New data formats can be implemented within the capabilities of the existing FEE hardware, with the goal to minimize dead time by a reduction of data volume. Two different approaches have been investigated:

- Tracklet Readout
- A significant readout time reduction can only be achieved by avoiding the handshaking overhead in the raw readout mode and by transferring information exclusively via the four data words associated to each MCM.
- In this mode the event readout time is in the range of  $4 \ \mu s$  up to around  $8 \ \mu s$  limited by the maximum number of words available in this readout mode.

The most stringent constraint is the limitation to 4 32-bit words (128 bits) per MCM which limits the acceptable local occupancy. Currently, in the tracklet mode one MCM can send up to four tracklet words, each with the following information: *z*position (longitudinal) in units of padrow (4 bits), *y*-position (transverse) in units of 160  $\mu$ m (13 bits), *y*-deflection (transverse) in units of 140  $\mu$ m (7 bits) and PID information (8 bits).

- In order to extend the charge information used for PID, the readout of 3 tracklets
   with 18 bits for PID information, or 2 tracklets with 40 bits for PID is foreseen. The
   bin widths for the positions would remain unchanged. Two charge slices are avail able directly from the preprocessor without additional delay, more slices could be
   calculated in the CPUs by looping over the data in the event buffers.
- Partial Data Readout

Another option to reduce the amount of data is a *partial raw data readout* in the raw 1386 readout mode. The readout can be restricted without information loss to regions 1387 where TRD information is relevant, i.e. only ADC data belonging to tracklets which 1388 fulfill a simple criterion for electron candidates. The selection of regions for readout 1389 has to be implemented within a MCM, based on a simple criterion optimized for 1390 data reduction and not necessarily for purity. A data volume reduction by a factor 5 1391 can be achieved; more studies are needed especially to evaluate the effect on track 1392 propagation from the inner detectors. 1393

Running with alternative data formats requires only a change of FEE configuration. Therefore new formats can be tested and optimized with real data throughout Run 2 without major disturbance for normal data taking. Depending on the rate requirements, either
 tracklet readout or partial data readout could be used in different running periods.

### 1398 Front-end read-out rates with new data formats

The readout rate performance of the new data formats is shown in Tab. 8.1 for the case of *Pb-Pb* collisions which constitute the biggest challenge for the readout given the large event sizes at comparably high interaction rates of 50 kHz or above.

<sup>1402</sup> Cases for the tracklet readout are shown for the maximum event readout time of 8  $\mu$ s and <sup>1403</sup> another more typical value of 6  $\mu$ s. Accepted event rates in the range of 60 kHz can be <sup>1404</sup> achieved for 100 kHz interaction rate, which is significantly higher than the accepted rates <sup>1405</sup> for any data format using the raw readout mode of the FEE.

<sup>1406</sup> In all readout scenarios with reduced or tracklet data the data volume is below 14 Gb/s/sector.

	interaction rate [kHz]	Accepted rate [kHz]	Accepted fraction [%]	deadtime [%]	data vo- lume
					[Gb/s/sector]
tracklet readout only					
avg. deadtime $6 \ \mu s$	50	38.5	76.9	23.1	4.73
	100	62.5	62.5	37.5	7.68
	200	90.9	45.5	54.5	11.17
avg. deadtime $8 \ \mu { m s}$	50	35.7	71.4	28.6	8.78
	100	55.6	55.6	44.4	13.65
partial raw data readout	50	23.3	46.5	53.5	7.8
full zero-suppressed ADC data	50	16.6	33.2	66.7	27.9

Table 8.1: TRD readout rates and data volume for different TRD data formats and event scenarios.

For the given readout rates and data volumes, a Pb-Pb minimum bias raw event size of 1407 210 kB/sector (28.3 kb/event/link) is assumed, derived from the experimental value of 1408 170 kB/sector (2011 *Pb-Pb* data at  $\sqrt{s_{NN}} = 2.76 TeV$ ) and scaled to  $\sqrt{s_{NN}} = 5.5 TeV$ . 1409 For the tracklet event size, occupancies of 25% (6  $\mu s$  case) and 50% of the maximum 1410 number of tracklet words (8  $\mu s$  case) are assumed. For the partial raw data readout, a 1411 factor 5 of data reduction with respect to the full zero-suppressed ADC data is assumed. 1412 The numbers of accepted events are estimated based on FEE readout time and interac-1413 tion rate only. 1414

Possible rate limits coming from the increased power consumption at the upgrade readout rates were investigated in test runs where tracklets were produced artificially by adjusting the FEE baseline and cluster thresholds. Only the digital 1.8 V low voltage channels, which are used for components in the FEE chip that are clocked exclusively during event processing, show a significant dependence on readout rate. Measured currents are below 150 A for all running scenarios up to 100 kHz readout rate, well below the 200 A current limit of the LV supplies.

### 8.3 TRD Performance with new data formats

The TRD currently calibrates gain, drift velocity  $v_d$ ,  $E \times B$  effects and time-offset; about 1422 30000 pp or 1500 Pb-Pb minimum bias events are needed to achieve a calibration point. 1423 The existing calibration procedures can be preserved with the new data formats by read-1424 ing the full zero-suppressed ADC data instead of the tracklet words for a small subset of 1425 events, with negligible effects on deadtime and data volume. It is also conceivable that 1426 calibration could exclusively use tracklet words, doing gain calibration with the charge 1427 information available in the tracklet words and integrating other calibration parameters in 1428 a global alignment procedure. 1429

As a conclusion the tracklet readout scenario would allow - with the existing FEE hardware - to read-out more than 70 % of events at the envisaged *PbPb* minimum-bias 50 KHz interaction rate including also the TRD detector. A study on the impact on tracking and particle identification performance of the new format is presented in the next section.

### **8.3 TRD Performance with new data formats**

The performance for tracking and PID of the reduced information content of the tracklet readout scenario described above is assessed by comparing it to the performance of the offline reconstruction based on full zero-suppressed ADC data (ZS) (for details see [48]) and TPC seeding. Results from *pp* data at 8 TeV (production LHC12f) are presented for the two tracklet reconstruction scenarios:

• read-out tracklets obtained *online* as currently used for trigger purposes

• tracklets calculated *offline* from ZS data with an improved PID content.

Their matching was done with respect to corresponding global tracks by their azimuthal and polar positions at the radial distance of the anode wire of the corresponding TRD chamber. The offline residual misalignment is applied in both cases.

The tracklet reconstruction efficiency for online relative to offline scenarios is presented in Fig. 8.2 (left) for a single *pp* run. Due to systematic effects induced by drift being perpendicular to magnetic field deflection (E x B effects) positive and negative charged particles are influenced differently. They are therefore shown separately in order to assess the  $p_T \sim 1.5 \ GeV/c$  threshold above which reconstruction is not affected by particle charge. From Fig. 8.2 (left) we conclude that the TRD contribution to global tracks should remain unchanged within 4 % when using the tracklet read-out format.

The quality of TRD reconstruction for track position in the azimuthal plane with respect to global tracks is presented in Fig. 8.2. The residuals ( $\Delta y$ ), obtained chamber-wise, are characterized by Gaussian shapes with comparable sigmas, *i.e.* resolutions (Fig. 8.2 right) for both tracklet reconstruction scenarios. The TRD tracking performance remains unchanged for positive particles above  $p_T \sim 1.5~GeV/c$  and for negative particles above  $p_T \sim 0.8~GeV/c$ .

The online tracklet performance at low  $p_T$  develops asymmetrically with particle charge due to the missing correction for the ion tails (Tail Cancellation - TC).



Figure 8.2: TRD reconstruction performance relevant for tracking. The reconstruction efficiency of online relative to offline (left) and the quality of azimuthal residuals ( $\Delta y$ ) resolutions (right) for positive [red] and negative [blue] charged particles for the two tracklet reconstruction scenarios.

<sup>1460</sup> Characteristics relevant for particle identification of the estimation of the track angle, in a <sup>1461</sup> single TRD chamber, by the two tracklet scenario are presented in Fig. 8.3 (right). The <sup>1462</sup> Gaussian shaped residuals ( $\Delta\phi$ ) are described by shifts with larger values obtained for <sup>1463</sup> the online tracklets are due mainly to missing TC corrections and also to limited calibration <sup>1464</sup> precision for drift velocity and  $E \times B$  effects.



**Figure 8.3:** TRD reconstruction performance relevant for particle identification. The online [open symbols] tracklet scenario, trigger tuned and normalized,  $\pi$  efficiency for 75% electron efficiencies and the corresponding ofline [filled symbols] performance for particles registered in 6 TRD layers (left) and the characteristic shifts of angular residuals ( $\Delta \phi$ ) in the bending plane for positive [red] and negative [blue] charged particles for the two tracklet reconstruction scenarios.

In the left panel of Fig. 8.3 the particle identification (PID) performance is compared for
 online reconstructed tracklets optimized for triggering and normalized to global track incli nation and offline tracklets respectively. The pion efficiency at 75% electron efficiencies
 for the online scenario is projected on the much higher statistics offline data set using a

### 8.4 TRD readout and trigger

normalization factor of 15 %. The target 1% pion efficiency at 2 GeV/c momenta will be reached at 75% electron efficiency.

<sup>1471</sup> The identification of particle species is in this case done offline based on reconstructed <sup>1472</sup> secondary vertices ( $V_0$  candidates) due to photon conversion,  $K_0$  and  $\Lambda$  decays. It is <sup>1473</sup> worth to note that the TRD 1-dimensional PID is formed out of two ingredients, the total <sup>1474</sup> charge and the track inclination. For online tracklets PID and inclination (local momentum) <sup>1475</sup> can not ne optimized simultaneously. Rather, PID can be best calculated after global <sup>1476</sup> tracking is performed using the good online position information. For the upgrade data <sup>1477</sup> without TRD electron trigger this poses no limitation.

### 1478 8.4 TRD readout and trigger

### 1479 8.4.1 TRD readout unit

In the following paragraphs the specifications for a new TRD readout unit are presented
 (see also Fig. 8.4). The major upgrade is the higher bandwidth interface to the DAQ: the
 full minimum bias triggered FEE data stream has to be transferred instead of the full zero suppressed ADC data for a small subset of L1 accepted events, as in the GTU modules
 that currently implement the TRD readout functionality [49].



Figure 8.4: Block diagram of the TRD readout unit.

The expected data volume per sector is below 20 Gb/s (see Tab. 8.1). This translates into two readout units (RU) per TRD sector, each with one 10 Gb/s uplink to the DAQ first level processors (FLPs). The RU has 30 optical input links, each transferring data from the FEE of one TRD half chamber at a net data rate of 2 Gb/s. In case of tracklet readout, the data transfer from the FEE is active for less than 12% of the time for all scenarios shown in Tab. 8.1. Together with the 5 times higher bandwidth of the DAQ link, the 30:1 ratio of FEE input links and DAQ output link on one RU is adequate. The RU must be able to handle different event types: (A) tracklet data (B) full zerosuppressed raw events for calibration, (C) partial raw data and (D) full *non zero-suppressed* events (not in physics runs). Tab. 8.2 shows event sizes and buffer requirements for typical cases of the various event types.

Event type	data volume kB/event/sector	data volume kb/evt/input link	number of events in 512 kb link buffer
50% tracklet words (A)	30.8	4	128
minimum bias raw (B)	200	27	19
central raw (B)	pprox 700	100	5
minimum bias partial (C)	40	5.4	95
non zero-suppressed raw (D)	pprox 3000	400	1

Table 8.2: Event size and RU input buffer capacity for various event types.

The input buffers on each FEE link act as multi event buffer (MEB) for the readout. The 1496 FEE data transfer to the RU uses a pure push mechanism without handshake or BUSY. 1497 To avoid data loss during this transfer, the RU input buffer size and bandwidth have to 1498 be large enough to accept at least one event of maximum possible size simultaneously 1499 on all links. The largest possible event type, a non-zero suppressed raw event, requires 1500 a buffer size of 400 kb. This size allows the storage of a sufficient number of events for 1501 all event types in physics runs as shown in Tab. 8.2. With e.g. 512 kb link buffers, the 1502 single buffer can equally hold five central raw events or 64 events with maximum number 1503 of tracklets using a dynamic event buffer size. 1504

For the interface to the DAQ there are no specific requirements from the TRD. Any chosen common ALICE DAQ link can be implemented for the TRD readout with the choice of a suitable FPGA device. The goal for the TRD readout is to use the ALICE common readout unit (CRU). The scheme of 30 FEE optical links inputs and 1 DDL output maps to one AMC40 card.

The CRUs for the TRD are ideally located in the counting room, allowing full accessibility 1510 during data taking. Alternatively, the CRUs can be installed in the current GTU racks in 1511 the C-area, re-using the existing fibers from the TRD supermodules to the GTU (1044 1512 fibers) and from the GTU to the DAQ area. In the C-area the level of radiation is not a 1513 concern for the CRU. Besides the impact on cost for the extension of 1044 optical fibers 1514 to the counting room for the first option, the feasibility in terms of the optical power that 1515 can be driven by the FEE for the extended optical links and with the additional multi-fiber 1516 push-on (MPO) connectors (see Fig. 8.4) for both options has to be evaluated carefully. 1517

### 1518 8.4.2 Trigger and busy handling

For operating the TRD, trigger sequences need to be provided to the FEE and in parallel to the CRUs. The FEE mounted on the detector chambers will remain unchanged for the upgrade, employing a TTCrx device to receive and distribute trigger information to all FEE devices. Therefore a TTC system for trigger distribution is needed for the TRD. The FEE requires a special trigger sequence on the TTC A-channel, which is not compatible with

### 8.4 TRD readout and trigger

the standard TTC trigger sequence. It consists of individual pulses one bunch crossing wide with a fixed timing for each provided trigger level. No TTC trigger messages are used on the FEE, thus no rate limit is imposed by using the TTC at high rates for the TRD.

For the TRD FEE, a single trigger level (LM) is sufficient to initiate the full processing and readout sequence. The timing of the LM signal has to be identical to the current TRD pretrigger with an arrival time at the FEE of, at the latest, 900 ns after the interaction in order to record the full signal shape including the early amplification peak. The FEE supports up to two additional trigger levels: a L0 or L1 trigger, which, in case of tracklet readout mode, is faster than 4  $\mu$ s can abort the FEE processing and thus reduce the dead time for L0 or L1 rejected events.

<sup>1535</sup> The CRUs receive a full standard trigger sequence including trigger messages which are <sup>1536</sup> used for BUSY generation and event formatting.

The CRU generates the TRD BUSY signal for the CTP. Each CRU asserts BUSY upon arrival of an LM trigger and releases the BUSY as soon as event end-markers are received on all FEE links or a time-out occurs. Moreover BUSY is asserted in case of full buffers.

### 1541 8.4.3 Schedule, funding and institutes

<sup>1542</sup> Table 8.4, 8.5 and 8.3 shows the TRD schedule, funding and institutes.

Contributing Institutes
University of Frankfurt, Germany
Gesellschaft für Schwerionenforschung, Darmstadt, Germany
University of Heidelberg, Germany
University of Münster, Germany
NIPNE Bucharest, Romania
Tokyo University, Japan

#### Table 8.3: TRD institutes.

Schedule		
New data	2015-17	test runs with with beam (pp, Pb-Pb); performance
formats		evaluation and optimization of data content
	2016-18	modification of software (offline reconstruction,
		calibration, data quality monitoring)
Readout unit	2015-17	firmware development and tests with prototypes
	2018	commissioning of all units

 Table 8.4:
 TRD schedule.

Funding				
Readout unit	36 CRUs, fiber connectors, crate, trigger & busy distribution	420 kCHF ( CRUs in C-racks)		
		additional cost for fiber routing to counting room		
Manpower	firmware and software development			
	2015-16	1 FTE		
	2017-19	2 FTE		
Besources for funding will be requested from BMBE				

Resources for funding will be requested from BMBF

Table 8.5: TRD funding.

## **Chapter 9**

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# **Time Of Flight detector - TOF**

### 1545 9.1 Introduction

<sup>1546</sup> We discuss the implications of the increased interaction rate at ALICE after the upgrade <sup>1547</sup> and the new requirements for the readout for the TOF detector.

During run 1 the current of the MRPCs increased linearly (Fig. 9.1-left, taken from [50]) 1548 with the LHC luminosity: abnormal noise current was not observed. Taking into account 1549 the average track multiplicity and the ALICE interaction rate, the two horizontal axes were 1550 aligned to the same detector load (number of particles hitting the TOF). Considering 1551 again the interaction rate at ALICE and the TOF hit multiplicity per event we estimated 1552 the average rate of particles in the detector as a function of the total TOF current. This is 1553 shown in Fig. 9.1-right (again taken from [50]) and we observed a maximum average TOF 1554 rate of 14 Hz/cm<sup>2</sup>. From the two plots in Fig. 9.1 it is possible to extrapolate the TOF rate 1555 to the luminosity foreseen in the ALICE upgrade beyond 2018. The expected rates will be 1556 60 Hz/cm<sup>2</sup>: test beam results [51] indicate that also in the high-luminosity LHC period the 1557 MRPCs will be able to operate without loss in performance. From Fig. 9.1-right it is also 1558 possible to compute an average induced charge of  $\approx 6 \text{ pC}$  per track. This value is slightly 1559 higher than what was obtained in test beam [52], but still compatible. The difference 1560 depends on the fact that in ALICE the particles are of different species and cross the 1561 MRPC at different angles and with different momentum spectra. This low charge ensures 1562 a good rate capability and protects the detector from aging [51]. Further details can be 1563 found in [50]. 1564

The present TOF readout can already cope with triggers of tens of kHz. For the ALICE upgrade program the main aim will be to further increase the present limit up to the minimum bias trigger both in pp and *Pb-Pb* interactions. As explained in the Letter of Intent, this can be achieved without major modification of the present hardware. A continuous readout would be instead unaffordable both for hardware and budget reasons.

<sup>1570</sup> In the following the TOF readout will be briefly reviewed and the main hardware and <sup>1571</sup> software modifications for the upgrade will be described. With respect to what was antici-



Figure 9.1: Left: the TOF current versus luminosity in Pb-Pb and p-Pb. Right: the TOF estimated rate versus HV current. In both figures the points and the bands indicate the average and the spread of the measurements, respectively. The dashed line is the linear fit to the 2013 data.

pated in the Letter of Intent, and consistently with the ALICE trigger strategy discussed in
this report, we no longer foresee any update of the existing TOF trigger capabilities. For
the upgrade the TOF trigger will be used only for commissioning purposes to provide a
cosmic trigger to central barrel detectors.

### **9.2 TOF present readout and limitations**

The existing TOF readout [53] is shown in Fig. 9.2. Each of the 18 azimuthal sectors of ALICE houses a TOF SuperModule, which is readout by 4 electronics crates. In each crate 1 DRM (Data Readout Module) collects the data of 10 TRMs (TDC Readout Module) [54], each of them including 30 HPTDC [55, 56] chips: 2400 channels are read-out in each crate. The pipelined internal architecture of the HPTDC chips coupled with readout buffers in the TRMs allows a zero dead-time readout.

- <sup>1583</sup> The readout is done in three distinct phases:
- HPTDC readout: the readout of HPTDC chips internal buffers and shipping of data to TRM internal memories.
- VME readout: the readout, over the VME bus, of the 10 TRM cards;
- DAQ readout: the shipping of data from the DRM to the ALICE Central DAQ over a DDL link;

In terms of DDL links data segmentation is equal to the number of crates, that is 72. At L1 arrival ( $\approx 6 \ \mu s$  after collision) a trigger is sent to the HPTDC and at the L2 arrival ( $\approx 80 \ \mu s$  after collision) the TRMs are read-out.



Figure 9.2: Current readout TOF scheme.

<sup>1592</sup> The existing limitations of the current scheme were discussed in the Letter of Intent and, <sup>1593</sup> extensively, in [57].

In short, the system which was operated during run 1 was limited by several factors, in-1594 cluding the amount of DAQ LDCs serving multiple TOF DDL links and the servers used 1595 for that purpose. In practical terms the readout was limited to some tens of kHz, already 1596 close to the foreseen targets for ALICE upgrade in PbPb runs. These limitations will be 1597 removed in the new DAQ scheme and are no more considered. The system analysis 1598 showed that the readout time of the HPTDC chips inside TRM cards sets a 440 kHz 1599 upper limit for the absolute maximum trigger rate that can be sustained by the TOF. Re-1600 placement of these cards (and of the HPTDC chips) is neither advisable or feasible and 1601 it is therefore not planned. 1602

Between the maximum theoretical achievable rate and present DAQ limitations, subse-1603 quently additional bottlenecks come from the data transfer speed over VME (currently  $\approx$ 1604 40 MB/s), the data size of almost empty events (which are the majority in pp collisions), 1605 the current trigger dispatch protocol and the performance of DDL links with small size 1606 payload per event. Potentially a hardware upgrade of the existing readout card might not 1607 be strictly needed because a 50-100 kHz sustained rate could be reachable only upgrad-1608 ing the firmware but this would limit the TOF contribution in pp runs and it would not allow 1609 the exploitation of the new DDL and TTS link capabilities. 1610

In the Letter of Intent we explained planned further work to study and curb these limi tations would have been done towards the preparation of the present TDR. Results and
 work in progress are presented in the next section together with the conceptual design of
 the foreseen new readout card.

### **9.3 Upgrade implementation architecture**

The ALICE DAQ group performed rate tests with upgraded DAQ cards (DDL RORC over PCIe) and updated mother-boards with respect to those used at ALICE during run 1. On the sending side a test bench card similar to the on-detector part of the DDL, the custom source interface unit (SIU), which is comparable to the current version installed in TOF DRM cards was used to check maximum achievable rates with an event size comparable to the foreseen payload from TOF crates ( $\approx$  200 bytes): rates up to 400 kHz have been reached, making it clear that the TOF will not suffer limitations from the DAQ bandwidth for the upgrade. The installation of DDL 2 or DDL 3 links on the new DRM cards will further avoid any bottlenecks on this respect.

The data segmentation will remain the same (ie. the whole TOF is read-out via 72 DDL links, each corresponding to the readout of a VME crate). The data format of the control words of each TRM (currently 24 bytes) will change and it will be reduced to 8 bytes when no hits are present. As discussed in the Letter of Intent this will greatly reduce the payload/event and the requirements on the VME bandwidth to be achieved. We foresee to deploy upgraded firmware already for run 2. New data format is described in Fig. 9.3.



**Figure 9.3:** New data format for control words sent by each TRM. Headers and trailers of each chain of 15 HPTDC data will be dispatched only if at least one hit is present otherwise they will be suppressed. Status bits S0 and S1 will allow to check data suppression worked correctly. This approach will reduce by a factor three the data size to be transferred over VME bus for 'almost empty' events, which are the dominating ones operating with a minimum bias trigger as foreseen in run-3.

<sup>1631</sup> The foreseen data size per DDL link will depend on event multiplicity. For almost empty <sup>1632</sup> events (in minimum bias events in pp collisions 50 hits/event are expected in the full TOF) <sup>1633</sup> this will be  $\approx$  140 bytes growing up to  $\approx$  1200 bytes for most central collisions in PbPb.

Internal HPTDC buffers allow to comfortably wait, with zero dead-time, for the L1 trigger. 1634 There is no need for TOF to deliver L0 to its FEE, also because a reject signal (e.g. L0 1635 not confirmed by L1) would force however the need to read all HPTDCs and then discard 1636 the data. Upon L1 reception the signal will be passed to HPTDC and VME readout will 1637 start immediately after they are made available on the readout FIFOs inside the TRMs. 1638 It is important to note this is currently done when awaiting the L2 accept signal, so this 1639 does not really add to the readout time. In run-3 this will be different. Besides the already 1640 discussed time to scan and read-out HPTDCs (could be up to  $\approx 3 \ \mu s$  depending on 1641 multiplicity as discussed in [57]), the time transfer over VME will determine the final TOF 1642 maximum achievable rate. 1643

To improve the VME throughput over the backplane, we plan to take advantage of the fact all VME cards (master and slaves) work on the same LHC clock. This can be exploited particularly implementing a synchronous protocol as the 2eSST VME standard. On the other hand we are limited by the existing hardware (both FPGAs and VME bus transceivers) mounted on the VME slave cards. The implementation of a simplified 2eSST protocol is envisaged, avoiding initial rate negotiation as foreseen by the origi-

### 9.3 Upgrade implementation architecture

nal industrial standard [58]. The theoretical achievable throughput, limited by the per formance of existing VME slave cards, is 160 MB/s, but the actual rate depends also
 crucially on the time spent during the initial data transfer phase (asserting addresses on
 the backplane).

Taking together the set of these results and developments, we can therefore confirm that the only hardware intervention to make the TOF fitting for the upgrade purpose will be the production of a new DRM card.

In front of a relatively small investment, the TOF will gain greater benefits upgrading its 1657 DRM card. This will allow to reach higher rates (likely around 300 kHz) which will ensure 1658 that in a short time a high statistic sample can be acquired in pp collision with events 1659 having ITS, TPC and TOF read-out. The benefits for ALICE physics program are evident. 1660 Moreover this hardware upgrade will allow the use of more modern TTC and DDL links, 1661 including a better handling of the busy signal over the new TTS system implemented 1662 using GBT links. Even if the multibuffer system - built-in inside the HPTDC architecture -1663 allows the TOF to safely handle many triggers, the busy will need to be dispatched with 1664 minimal latency (O( $\mu$ s)) to protect against FIFO overflow and other potential busy reasons 1665 (DAQ not coping with data and some VME cards not ready). With a new DRM card we 1666 might further expect some benefits on the 2eSST obtainable performance (that is a 160 1667 MByte/s bandwidth) improving the hardware of bus transceivers on the master card. This 1668 is not guaranteed however because, as discussed, the hardware of the VME slave cards 1669 will not be reviewed. 1670

<sup>1671</sup> Figure 9.4 shows the readout scheme after the foreseen upgrade.



Figure 9.4: New TOF readout scheme, with upgraded components highlighted.

Not all the actual technical implementation details of the new DRM card ("DRM2") have
been already defined, mainly due to the uncertainties about new hardware supporting
trigger and DAQ links. Production of prototype cards are expected to start in 2014 following availability of chosen standards.

<sup>1676</sup> A conceptual design layout of the card is shown in Fig. 9.5 and we list here some con-<sup>1677</sup> siderations and information about hardware choices and differences with respect to the <sup>1678</sup> existing card.

• a SmartFusion2 FPGA from Microsemi is the current favourite candidate for DRM2 and an obvious successor of the Actel APA750 currently used on the DRM. Being

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Figure 9.5: Conceptual design of new version of the TOF Data Readout Module

Flash programmed it provides SEU immune configuration cells and it has several built-in radiation tolerant features such as SEU protected memories. Interestingly this FPGA features high-speed serial interfaces (important to implement IP cores towards new TTC and DDL links) and an ARM CPU core. Given its capabilities are much higher than the current FPGA used in the DRM, we are very confident it will be able to replace the second FPGA (an Altera Cyclone) currently on board on the existing DRM, taking care of the slow control optical link;

- the Slow Control Link is used by the TOF DCS servers to monitor and configure Front End Electronics. It is additionally used to collect spy data during data taking for control of data consistency and monitoring of several DCS parameters (namely temperatures and thresholds). The memories shown in the Fig. 9.5 are used to stage collected data in multi-events buffers for DCS transfers. This arrangement worked very well during run 1 and before run 2 the back-end links will be already upgraded to PCIe, similarly to what the ALICE DAQ did for D-RORC cards;
- the ARM processor was installed inside current DRM to provide remote programming of Actel FPGAs inside TOF VME cards, via a private JTAG bus implemented on the VME backplane. The current hardware, a commercial piggy-back card mounting an ARM Atmel processor running Linux, could be reused. We will explore however if the ARM core inside the Microsemi FPGA could be used for this purpose, simplifying the design of the card.
- for the TTS link a bi-directional GBT link is foreseen, used also to provide the busy signal to the Central Trigger Processor.
- The interface to the back-end DAQ will be a DDL 2 link as baseline option (no DDL 3 is foreseen in the cavern). The encoding will be again implemented inside the FPGA via an IP core provided by the ALICE DAQ group. The implementation of a

### 9.4 Schedule, funding and institutes

DDL 2 link on the new DRM will take advantage of the expertise gained by TPC and TRD groups during run 2 (a DDL 2 link is operating on the Readout Control Unit (RCU) for these detectors).

Radiation tests will be carried out as necessary with untested components once defined. We plan however to use largely the existing tested components on the DRM exploiting the know-how gained during DRM electronics development (with features like a watchdog microprocessor protecting against latchup). We will also rely on irradiation tests which are currently being carried out by other ALICE groups on SmartFusion2 FPGAs.

### 1714 9.4 Schedule, funding and institutes

<sup>1715</sup> A total cost of 600 kEU is foreseen for the production of the new DRM cards and related <sup>1716</sup> R&D costs (prototype cards, radiation tests, software licenses, test setup in laboratories, <sup>1717</sup> etc.). The foreseen upgrade schedule with spending profile is shown in Tab. 9.1.

Year	Activity	Cost [kEU]
2013	Firmware development (2eSST, data compression)	15
2014	Prototype card: testing new FPGA with GBT and new DDL links	35
2015	Finalization of specifications, radiation tests, tendering	50
2016	Start of production of DRM cards	250
2017	End of production	250
2018	Installation at pit and Commissioning	

 Table 9.1: TOF upgrade plan: spending profile is also shown.

<sup>1718</sup> The involved institutes in this project summarised in table 9.2.

### Institutes

sezione INFN and Dipartimento di Fisica dell'Università, Bologna, Italy sezione INFN and Dipartimento di Fisica dell'Università, Salerno, Italy Centro Studi e Ricerche e Museo Storico della Fisica "Enrico Fermi", Rome, Italy Gangneung-Wonju National University, Gangneung, South Korea

Table 9.2: TOF institutes.

## Chapter 10

# **Fast Interaction Trigger - FIT**

1721 10.1 Introduction

In the present ALICE detector there are three forwards detector systems, the T0 [59], V0 1722 [60] and FMD [61], that provide minimum bias trigger, multiplicity trigger, beam-gas event 1723 rejection, collision time for TOF, offline multiplicity and event plane determination. In order 1724 to adapt these functionalities to the collision rates of the ALICE upgrade, it is planned to 1725 replace these systems by a single detector system, called the Fast Interaction Trigger 1726 (FIT). Two sensor technologies are investigated for FIT. They represent improvements of 1727 the current T0 and V0 detectors. We refer to these modified detector components as 1728 T0-Plus and V0-Plus. While it would be possible to build the FIT based on only one tech-1729 nology, it might lead to loss of redundancy and partial reduction of functionality. We intend 1730 to investigate both sensor technologies concurrently and to develop front-end electronics 1731 suitable for both technologies. The readout system adopted for FIT will follow the scheme 1732 of the current T0 detector using the DRM and TRM modules developed for the TOF de-1733 tector. For this reason, even if FIT employs both sensor technologies, it will appear as a 1734 single detector system. 1735

### **1736 10.2 Performance of the current T0 detector**

The current T0 detector consists of two arrays of Cherenkov counters (T0-C and T0-A) 1737 positioned at the opposite sides of the Interaction Point (IP) at distances of -70 cm and 1738 370 cm. Each array has 12 cylindrical counters equipped with a guartz radiator and a 1739 photomultiplier tube (see Fig. 10.1). T0-C covers the pseudo-rapidity range  $-3.28 < \eta < \eta$ 1740 -2.97 and T0-A covers  $4.61 < \eta < 4.92$ . Due to the small acceptance of the T0 arrays, 1741 the time resolution and efficiency of the T0 detector improve considerably with event 1742 multiplicity. For instance in pp collisions, T0 system achieves a 40 ps time resolution 1743 and 50% vertex efficiency. For central and semi-central events (centrality range 0-60%) 1744

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Figure 10.1: Conceptual drawing of the trigger detectors on the C-side as they are now (left) and after the upgrade (right). The new T0-Plus detector will consist of 20 rectangular modules. Although the upgraded V0 detector will have a modified light collection system, the area covered by the scintillator would remain the same.

<sup>1745</sup> in PbPb collisions at  $\sqrt{s_{NN}}$  = 2.76 TeV, the corresponding values are  $\sim 21 \text{ ps}$  for time <sup>1746</sup> resolution and close to 100% for vertex efficiency, as shown in Fig. 10.2.

#### 1747 **T0 electronics**

The block diagram of the electronics and readout scheme used by the present T0 detector 1748 is shown in Fig. 10.3. The signals of each of the 24 PMTs are fed to preamps housed 1749 in the so-called shoeboxes, placed at 6 meters from the detector. The main reason for 1750 the shoebox was to provide the wake-up signal for the TRD, however this will be derived 1751 in a different way already after LS1. Nevertheless, because of the considerable distance 1752 between the photo-sensors and the electronics racks, where the fast electronics will be 1753 located, we envisage the first stage of signal amplification at a distance of no more than 1754 3 m from the detector. From the shoebox, the signals are sent to the trigger and readout 1755 electronics located in the racks outside the magnet. The fast trigger electronics includes 1756 processing of the PMT signals, generation of the required trigger signals and shaping for 1757 digitization and storage by the TRM and DRM modules. 1758

The readout electronics processes, digitizes, and sends for storage the arrival time and amplitude from each of the photo sensors. The main components of this system are custom VME crates (SY2390), the TRM (TDC Readout Module), the CPDM (Clock and Pulse Distribution Module) and the DRM (Data Readout Module). All these components



**Figure 10.2:** Performance of the current T0 detector for PbPb collisions as measured in 2011. Top left: Distribution of (T0A-T0C)/2 corrected for slewing and vertex. Top right: Distribution of the interaction time measured by T0. Bottom left: Background rejection by T0. Bottom right: T0 vertex trigger efficiency for central and semi-central collisions (0-50%).

are equivalent to the ones developed for the TOF detector. The same general architecture, with an increased channel number, will be used by FIT.

### **1765 10.3 Performance of the current V0 detector**

The V0 system consists of two discs at distances of -90 cm and 329 cm from the IP and cover the pseudo rapidity-ranges  $2.8 < \eta < 5.1$  and  $-3.7 < \eta < -1.8$ . The two detectors are segmented in four rings and 8 sections in the azimuthal direction. The system is made of plastic scintillator from Bicron and light is collected with WLS fibers embedded in both faces of V0-A or glued along the radial edges of V0-C.

The V0 systems generate two types of trigger signals. One type is based on pre-adjusted time windows that corresponds to beam-beam or beam-background in coincidence with the time signals from the detectors (see Fig. 10.4 left). This is used for minimum bias, beam-gas and multiplicity triggers. The second type is based on total charge and is used to trigger on multiplicity.

The V0 system also provides on-line monitoring of the luminosity and background rates using a time coincidence between the two V0 arrays.

A typical distribution of V0 amplitudes used for centrality selection is shown in Fig. 10.4



Figure 10.3: Trigger and readout electronics of the present T0 deteector.

(right). Fig. 10.5 (right) shows the resolution of the event plane as determined by the V0.

### 1780 V0 electronics

The 32 channels of each V0 detector are received by a FEE that splits each PMT pulse into two. One is fed into charge-to-digital converters to integrate the charge. The other is amplified by a factor 10 and provides the leading edge timing as well as the width at the discriminator threshold. The time information of both leading edge and width is digitized by time-to-digital converters.

The block diagram in Fig. 10.6 shows the concept of the present V0 readout [63]. The shoebox in the diagram provides the wake up signal to the TRD. It is one of the features that will disappear in the future system. The Channel Interface Unit (CIU) performs charge and time digitalization. It contains an HPTDC that gives a precise time information for 8 channels i.e. one ring of V0. The CCIU performs the interface function between the DAQ and the electronics as well as the final processing of the trigger signals.



**Figure 10.4:** Left: Time of flight distribution of V0-A and V0-C obtained with pp collisions after a weighted average [60]. The RMS value of the distributions are 450 ps and 350 ps respectively. Right: The sum of amplitudes in lead-lead collisions at  $\sqrt{s_{NN}}$ =2.76 TeV. The red line shows the Glauber model. The shaded areas define centrality classes [60].



**Figure 10.5:** Left: Resolution of the centrality determination by different ALICE sub-systems [62]. Right: Resolution on the event plane determination with the V0 for the second harmonic as a function of the centrality percentile.

### 1792 10.4 Required functionality for the FIT

<sup>1793</sup> The upgraded trigger detector needs to fulfil the following requirements:

- Minimum Bias trigger for pp collisions with efficiency comparable to the current V0, i.e. at least 83% for vertex (A&C) and 93% for the OR signal (A|C).
- Event Multiplicity determination capable of selecting and triggering on central as
   well as on semi-central collisions. The centrality selection should match the performance of the present V0.
- Vertex location with a performance comparable to the present T0 system
- Evaluation and rejection of beam-induced background and in particular beam gas
   event sensitivity on the level of the current V0 detector.
- Time resolution better than 50 ps for pp collisions, as in the present T0 system.
- Determination of collision time for TOF with resolution better than 50 ps.



Figure 10.6: Block diagram of the present V0 readout electronics.

- Event plane determination with a precision similar to the present V0 system (see Fig. 10.5)
- Minimal ageing over the ALICE operation period.
- No after pulses or other spurious signals.
- Direct feedback to LHC on luminosity and beam conditions.

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### 1810 10.5 TO-Plus detector concept

The most natural approach to address the above requirements would be to increase the acceptance of the current T0 detector to match that of the V0. Using the present setup of a quartz+PMT is however impractical and not cost effective. Instead, a new concept with quartz radiators coupled directly to MCP-PMT based light sensors is proposed. Fig. 10.1 shows a sketch of 20 rectangular modules of such a detector at a position between the current T0 and V0.

### **10.5 T0-Plus detector concept**

### 1817 MCP-PMT technology

An MCP-based trigger detector was considered in the 1990's, during the initial planning and construction phase of ALICE. At that time this technology was not selected, as its long-time reliability had not yet been established. Since then, rapid progress has been made, driven primarily by the demand for MCP-based night vision devices for the military. The most significant developments were:

- Atomic Layer Deposition technology [64]
- Modified photocathodes [65]
- Reduced outgassing (borosilicate glass)
- Commercially available self-contained MCP-PMT units

There are currently three producers capitalizing on these developments: Hamamatsu (Japan), Photonis (USA), and BINP (Novosibirsk in Russia). According to our recent (June 2013) market survey, the most suitable module for the trigger upgrade is XP85012 Planacon from Photonis.

### 1831 XP85012 Planacon

The XP85012 Planacon consists of a sealed, rectangular vacuum box of about  $59 \times$ 1832  $59 \times 28 \text{ mm}^3$  housing a pair of microchannel plates in a chevron configuration [66]. The 1833 pore size is  $25 \,\mu$ m with the length to diameter ratio of 40:1. There are two front window 1834 options available: Schott 8337B or UVFS(-Q). The spectral range is 200-650 nm with 1835 peak sensitivity around 380 nm and an average guantum efficiency of 22%. A gain of 1836  $10^5$  is typically reached at 1800 V, with the maximum possible gain on the order of  $10^7$ . 1837 The cathode is subdivided into 64 square sections that can be read out individually or 1838 combined into bigger blocks. Both the ambient operating temperature range and the 1839 behaviour in the magnetic field conform to the ALICE conditions inside the L3 magnet. 1840

<sup>1841</sup> Planacon has the largest relative (80%) and absolute (53 mm  $\times$  53 mm) active area and <sup>1842</sup> the lowest price per surface of all the commercially available MCP-PMTs, making it the <sup>1843</sup> prime choice for the T0 upgrade. The same product has been selected for the timing <sup>1844</sup> detectors for PANDA [67] at FAIR in GSI and for NICA [68] in Dubna. Both projects <sup>1845</sup> have already conducted significant R&D on this detector, which allows us to build on their <sup>1846</sup> results. Some of the test results shown in this chapter were obtained by the PANDA and <sup>1847</sup> NICA collaborations.

### **Reliability and lifetime issues**

Electrons multiplied by up to seven orders of magnitude in avalanches inside the microchannels inevitably degrade MCP surfaces, limiting the lifetime of the device. Likewise,



Figure 10.7: Photograph of a front (window side) and rear view of XP85012 Planacon.

the positive ions traveling in the opposite direction in the strong electric field also cause 1851 the generation of intense secondary electron showers and additional damage to the pho-1852 tocathode. The ageing of an MCP is typically reported by plotting the Quantum Efficiency 1853 (QE) as a function of the Integrated Anode Charge (IAC). Before the advent of Atomic 1854 Layer Deposition technology, MPCs suffered a drastic decrease in QE already after an 1855 IAC on the order of 100 mC/cm<sup>2</sup>. The latest tests with the Planacon XP85012 show no 1856 signs of degradation even after IAC of  $\sim$ 5 C/cm<sup>2</sup> [69], as shown in Fig. 10.8. Hamamatsu 1857 is now developing an MCP-PMT that will also push the limit beyond  $\sim 5$  C/cm<sup>2</sup>. The new 1858 product is expected on the market in 2015 that is in time for the upgrade. 1859

A minimum ionizing particle (MIP) traversing a 20 mm thick guartz radiator generates 1860 about 1000 photons. The Quantum Efficiency (QE) of the Planacon QE, it is around 1861 10% hence 1000 photons from 1 MIP will trigger 100 avalanches. Typical gains in use 1862 are around  $10^5$ . With such a gain there are  $10^7$  electrons that reach the anode per MIP, 1863 corresponding to a charge of  $1.6 \times 10^{-12}C$ . Referring to Section 3, the total number of 1864 tracks will be around  $3 \times 10^{12}$  on the innermost sensors and thus the total charge is close 1865 to  $\sim$ 4.8 C/cm<sup>2</sup>. This value conforms to the already proven performance of PLANACON 1866 [69], giving us confidence that the new MCP-PMT units will perform well for the ALICE 1867 upgrade. 1868

#### 1869 After-pulses

A serious issue complicating the use of PMT-based detectors (including the current T0 1870 and V0) are after pulses. As can be seen in the left panel of Fig. 10.9, some 20-120 ns 1871 after the main pulse, after pulses with amplitudes of about 20% of the primary peak occur. 1872 This phenomenon is well known and is attributed to the acceleration of ions triggering 1873 secondary signals. For low-multiplicity events, that is when most of the primary pulses 1874 are generated by a single MIP traversing the radiator, this phenomenon is not a problem 1875 since the after pulses fall below the threshold of the discriminator. At higher multiplicities 1876 this is no longer the case. Since the amplitude of an after pulse scales roughly with 1877



Figure 10.8: Dependence of the Quantum Efficiency on the Integrated Anode Charge for a variety of MCP-PMT sensors measured by PANDA collaboration. The performance of the ALD treated samples from Photonis USA is shown by the top curves.

the amplitude of the primary pulse, at higher multiplicities one gets potential problems especially when there might be an overlap with signals from the previous bunch crossing.

<sup>1880</sup> The MCP-PMT investigated has not shown any detectable after pulses, as can be seen <sup>1881</sup> in the right panel of Fig. 10.9.



Figure 10.9: Oscillographs showing the shape of pulses from a PMT currently used by T0 detector (left graph) and from a XP85012 proposed for T0 upgrade (right graph). No after pulses are visible in the Planacon spectrum.

### 1882 Quartz radiators

The fragmented anode of the XP85012 makes possible to increase the granularity of the detector by dividing the quartz radiator into smaller segments (see Fig. 10.10). This is possible because the total internal reflection from the sides of the radiator segment directs all Cherenkov photons onto the photocathode directly under this segment. Such increase in granularity will improve the performance of the detector especially for high-multiplicity
 events.



Figure 10.10: Concept of T0 module with a quartz radiator divided into 16 elements. The dimensions are approximate and do not account for detector housing and electronics.

#### **Choice of quartz supplier**

Two possible suppliers of quartz material for the radiator have been identified: Gus-Khrustalnyi from Russia, the producer of quartz KU-1, and Heraeus of Germany, which produces SUPRASIL 1. The former material is used by the current T0. The latter has a slightly wider transmission band at very short wavelengths. Both are suited for the upgrade of T0.

#### 1895 Surface coating

Cherenkov light cones generated by MIPs entering perpendicular to the front surface of a 1896 radiator do not lose much intensity upon reflection from the sides because the conditions 1897 for the total internal reflection are fulfilled. To take advantage of this fact, modules of 1898 the current T0-C array are inclined to face the IP. When the entrance angle of charged 1899 particles increases, some of the light escapes from the sides of the guartz. It is, as yet, 1900 unclear if the space available for the upgraded T0 would be sufficient for tilting of the 1901 detector units towards the IP. If not, highly reflective coating of the radiator sides will be 1902 employed to minimize the light loss. 1903

Also, coating of the front surface should be chosen depending on the desired performance for particles traveling in the opposite direction. Without any coating the polished

### 10.5 T0-Plus detector concept

front surface of the radiator would still reflect a sufficient amount of light towards the photocathode to generate a peak of roughly 50% the normal amplitude. A properly selected
light absorbing coating would remove this peak completely, while a reflective layer would
bring the signal amplitude for particles traveling backwards closer to that of the normally
traversing particles.

Final decisions on segmentation, angles, and optical coatings depend, of course, on the outcome of detailed simulations and the results of beam tests using various possible configurations. In any case our aim is to design T0-Plus that will be also able to monitor and measure beam-gas events. This is definitely possible but some more R&D is needed to find the optimum solution that would both be sensitive to the background events and yet be able to discriminate against them. This is a new feature of T0-Plus as compared to T0.

### **Detector prototyping**

The results presented in here have been obtained with a prototype constructed by NICA collaboration (Fig. 10.11). Judging from the existing prototype the minimum thickness of the fully assembled and cabled module is estimated at  $\sim$ 10 cm. The sensor itself is  $\sim$ 3 cm thick, the quartz would be 1.5-2 cm, the PCB with front-end electronics attached to the sensor  $\sim$ 2 cm, and 1.5 cm in the front and 1.5 cm in the back to accommodate the bending angle and connector thickness of signal and electrical cables and optical fibers.



Figure 10.11: Prototype of a detector module based on XP85012. Part of the outside cover is removed to show the rear side of the sensor with front-end electronics attached. This prototype has the quartz radiator and the anode divided into 4 equal sectors.

### 1925 **Time resolution**

MCP-based devices are known for their very good timing properties. The tests conducted both by ALICE and the PANDA and NICA groups confirm the excellent performance of XP85012 in that respect as shown in Fig. 10.12. The Time-of-Flight resolution of 42 ps as measured with cosmic rays by a pair of MCP based detectors corresponds to a resolution of 30 ps for a single detector element. As expected, the upgraded T0 should therefore have the same or even better time resolution than the current detector.



Figure 10.12: Measured TOF resolution obtained with cosmic rays for various pairs of MCP-PMT sectors obtained with the detector prototype shown in Figure 10.11.

#### 1932 Efficiency

The intrinsic efficiency for a quartz radiator with an MCP-PMT detector is close to 100%. That means that every MIP traversing a full path inside of the quartz generates a proper signal that will be registered. However the geometric coverage of the detector unit is less than 100%. The ratio of active surface to the physical outline of the XP85012 is 80%. When the necessary housing and mechanical support is added, this ratio will drop to about ~75%, depending on final design details.

#### 1939 Weight

According to the manufacturer, the approximate weight of XP85012 is 128 g. The weight of the  $53 \times 53 \times 20$  mm<sup>3</sup> radiator made of fused quartz (~2.2 g/cm<sup>3</sup>) is approximately

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### 10.5 T0-Plus detector concept

<sup>1942</sup> 124 g. The board with electronics and cable connectors together with a protective cover <sup>1943</sup> would bring the total weight of one module to 400-500 g. Therefore, the weight of a 20 <sup>1944</sup> unit array would be about 8-10 kg plus the weight of the HV cables (total of 20), signal <sup>1945</sup> cables (total of  $4 \times 20 = 80$ ) and optical fibers ( $\leq 20$ ).

### 1946 Acceptance and shape optimization

The demand to maximize the efficiency for Minimum Bias events requires efficient coverage of the available space with detector modules. The envelopes defined by detector integration are a minimum inner radius of 50-60 mm and a maximum outer radius of 170-200 mm. The proposed detector configuration is shown in Fig. 10.13. Each MCP-PMT module will be divided into 4 equal parts by cutting the quartz radiator into 4 and arranging the 64 anode sectors into the corresponding 4 groups. As a result, each array on the A and on the C-side will function as  $20 \times 4=80$  independent detector units.



Figure 10.13: Proposed configuration and segmentation of 20 modules of T0-Plus detector around the beam pipe.

It is still to be decided whether to place the C-side T0-Plus detector on the front-absorber or on the so called 'cage' that supports the beampipe, ITS and MFT. Fixation on the front-absorber allows an inner radius of 50 mm but has the drawback that the detector is only accessible if the TPC is moved to the parking position. Fixation on the support cage allows an inner radius of only 60 mm, but would ease the access to the detector.

For the detector optimization, a round of simulations with an ideal geometry assuming a perfect ring detector was performed. In these simulations, various values for  $R_{min}$ , beam

	Α	С	A&C	A C
рр	@ 14	TeV		
<b>V0</b> *	0.88	0.88	0.83	0.93
T0-Plus*	0.89	0.89	0.84	0.94
R <sub>min</sub> =50 mm				
T0-Plus*	0.88	0.88	0.83	0.93
R <sub>min</sub> =60 mm				
T0-Plus	0.88	0.86	0.80	0.93
Detailed geometry				
R <sub>min</sub> =60 mm				
PbPb @ 5.5 TeV (b)	>13 fm	; 70-10	0% cer	trality)
T0-Plus	0.97	0.98	0.95	0.996
Detailed geometry				
R <sub>min</sub> =60 mm				

 Table 10.1: Efficiency comparison between the current V0 and the proposed T0-Plus. Asterisks indicates that the simulations were done using a simplified geometry.

pipe options, and placement along the beam axis were investigated. In addition, 15000 1961 events generated with PHYTHIA6 for pp collisions at  $\sqrt{s}$  = 14 TeV were projected onto the 1962 real geometry of T0-Plus: 20 MCP-PMT sensors with  $53 \times 53 \times 20$  mm<sup>3</sup> guartz radiators 1963 placed around beam pipe at 70 cm on the C side and 20 MCP-PMTs at 373 cm on the A 1964 side. On both side the distance from the center of the beam pipe to the outer edge of the 1965 sensor was  $R_{min} = 60 \text{ mm}$ . The same geometry was used for the simulation with HIJING 1966 of 8000 events of the most peripheral (b=13-20) PbPb collisions at  $\sqrt{s}$  = 5.5 TeV. For all 1967 calculations the standard beam pipe geometry (adopted for upgrade simulations) was 1968 used. Fig. 10.14 shows the simulated T0-Plus efficiency as function of primary particle 1969 multiplicity in pp collisions, where the average is around 235 with a very large spread 1970 around this number. Fig. 10.15 shows the efficiency as a function of the impact parameter. 1971 Tab. 10.1 summarizes the main results of the simulations. We can conclude that the 1972 performance of the T0-Plus detector is very close to the present V0 detector, as specified, 1973 and that the choice of the inner radius between 50 and 60 mm is not a critical issue. 1974



Figure 10.14: Simulated efficiency of T0-Plus detector as a function of primary particle multiplicity.



Figure 10.15: Dependence of the efficiency on the event centrality for PbPb collisions at  $\sqrt{s}$  = 5.5 TeV.

### 1975 **10.6 V0-Plus detector concept**

One of the advantages of the current ALICE trigger detector setup is the partial overlap in functionality between T0 and V0. It is desirable to maintain at least some of the present redundancy in the upgraded detector. A natural choice for a second detector subsystem would be V0-Plus. This would be a modified and improved V0, a plastic scintillator-based system with the frontend electronics integrated with T0-Plus and the readout complying with the TOF standard.

The existing V0 performed satisfactorily during LHC Run 1, with the exception of some issues due to after-pulsing. In the following, a new V0-plus is sketched which meets the requirements of the new run conditions, in particular the increased collision rates in pp and PbPb. The severe conditions expected require a new design providing better time resolution, a larger acceptance, and much smaller after pulsing. The V0 detector assembly will be composed of a small number of independent modules which will be easy to be replaced at a minimal cost.

The new system design must continue to deliver the trigger signals provided by the current V0, including the possibility of vetoing the background due to beam-gas interactions. Because of much larger acceptance, it will both extend and complement the functionality. The final design will be developed within the Fast Interaction Trigger group, to ensure the optimal functionality of the Fast Interaction Trigger detectors. Both T0 and V0 arrays are located on both sides of the interaction point [4] at small radial distance from the beam line. A similar geometry will be used for the upgraded detectors.

<sup>1996</sup> V0-Plus will supply fast time signals to the first level trigger and, in addition, will provide an <sup>1997</sup> off-line multiplicity measurement and determination of the reaction plane. The design goal for V0-Plus is to improve the time resolution by an order of magnitude as compared with the current V0 and approach the level of 200 ps, while maintaining a large acceptance and high efficiency for the Minimum Bias Trigger. Better time and amplitude resolution achieved by improving the light collection from the scintillator will also improve the beamgas background rejection capabilities of V0-Plus.

The default position of the V0-Plus arrays coincides with that of V0A and V0C. The new arrays will consist of 32 (V0C+) and 32 (V0A+) cells of BC408 scintillation plastic. On the A-side where the space restrictions are not critical, the light collection will be provided by fine mesh photomultiplier tubes coupled directly to the scintillator cells. On the C-side, the available volume will be restricted by the new Muon Forward Tracker (MFT).

### 2008 V0-Plus rapidity coverage

V0A-Plus will consist of 5 rings, i.e. one more than the present V0, in order to increase the acceptance and eliminate the rapidity gap of 0.8 units between the SPD and the present V0A (Fig. 10.16).The new ITS [7] will have a wider pseudo-rapidity coverage of -2.3 << 2.3. Extending the coverage of V0A-Plus to  $\eta = 2.2$  eliminates the gap and provides a small overlap for efficiency determination using an independent system. Such overlaps in the existing forward detectors have proven to be extremely useful.



Figure 10.16: In the present system (left) there is a pseudo-rapdity gap of 0.8 units between the Silicon Pixel Detector and V0A. Adding a ring of 0.6 units in pseudo rapidity would increase the acceptance and would even provide an overlap useful for testing and efficiency determination (right).

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The pseudo-rapidity coverage of V0-Plus also overlaps with the coverage of T0-Plus and the MFT, providing the ability to perform important cross checks for physics analysis. The pseudo-rapidity coverage is summarized in Tab. 10.2.

Rin	g	V0A-Plus		V0C-Plus	
		$\eta_{max}/\eta_{min}$	$ heta_{max}/ heta_{min}$	$\eta_{max}/\eta_{min}$	$ heta_{max}/ heta_{min}$
0		5.41/4.5	0.7/1.3	-3.7/-3.2	177.0/175.3
1		4.5/3.9	1.3/2.3	-3.2/-2.7	175.3/172.4
2		3.9/3.4	2.3/3.8	-2.7/-2.2	172.4/167.5
3		3.4/2.8	3.8/6.9	-2.2/-1.7	167.5/159.8
4		2.8/2.2	6.9/12.7	Additional r	ing only on A side

**Table 10.2:** Pseudo-rapidity coverage of the new geometry. V0A+ may have an additional ring to cover the<br/>gap between the Silicon Pixel Detector (SPD) and the present V0A.

Redundancy is particularly important on the C side where access is difficult and deficiencies or failure of any of the detectors in the region should be backed up with alternative solutions. The distance to the interaction point is less than 1 meter and access to the area requires a removal of the central detectors of ALICE and of the beam pipe.

### 2022 Photo sensor options for V0-Plus

Both a MCP-PMT and a fine mesh PMT as possible light sensors for the upgraded V0 are considered. The former has already been described in the T0 section above. The use of the same sensor would have many advantages, as it would fully integrate the fast trigger detectors already at that level. On the other hand, the same sensor technology would increase the vulnerability of the trigger to unforeseen long-term problems with the MCP-PMT solution. If the primary goal is redundancy, one should consider the use of traditional PMTs for V0.

The R7761-70 photomultiplier from Hamamatsu [9] has been tested and will be used after 2030 LS1 at the actual V0 system. It is a fine mesh phototube with good timing properties. 2031 It has a 38 mm diameter with 27 mm diameter effective area. The spectral response 2032 of this PMT ranges from 300 nm to 650 nm, and peaks at 420 nm. With this broad 2033 range response, the WLS cookie can be avoided, thereby improving the time response 2034 of the detector. The photocathode material is bialkali and there are 19 dynode stages. It 2035 can be operated at lower Voltage than the previously used 16 dynode stage PMT from 2036 Hamamatsu (R5946), reducing the after pulsing rate for similar gains. The rise time is 2037 2.1 ns and the transit time is 7.5 ns. The MCP from Photonis [60] PP0365G which has 2038 a guartz window and a single anode has been tested. It offers immunity from magnetic 2039 field, a fast response and very low time jitter. 2040

### **10.7 Common front-end and readout electronics for FIT**

As discussed earlier the T0-Plus and V0-Plus will use the same front-end and readout electronics. The system will be based on the present T0 detector using the TOF modules <sup>2044</sup> for data readout.

#### 2045 Front-end electronics

FIT will use the same general scheme of front-end electronics as that used by T0 (see Fig. 10.2 and Fig. 10.3). The main new element of the front-end electronics will be the modernized amplifier. Because of the high radiation levels, it will have to be located not directly on the sensor but several meters from it. In addition to the amplifier, there will be shapers, fan-ins and discriminators to prepare the signal to be sent to the electronics racks. Functionally, the electronics sketched in Fig. 10.17 will replace that currently in the Shoe-box (see Fig. 10.2).



Figure 10.17: Conceptual diagram of the new first stage of the front-end electronics for the FIT. This part will replace the current electronics depicted on Fig. 10.3 by the diagram labeled shoe-box.

#### 2053 Readout

Currently T0 uses only one DRM and one TRM. As FIT will have considerably more channels, the number of TRMs must be increased. Each TOF crate has 10 slots for TRMs. Going beyond that would require additional crates and services and, as a result, considerably increase the complexity and cost of the readout electronics. To avoid these complications the options that would limit the readout of FIT to one VME crate are investigated. This work is done in close collaboration with the TOF group who is also working on increasing the VME transfer rate.

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### 2061 **10.8 Funding**

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The most expensive items needed for the upgrade of the T0 detector are the new MCP-2062 PMT units currently valued at \$8500 each. Including the housing, guartz etc. it is reason-2063 able to estimate  $\sim 10$  kCHF for each assembled detector module. Therefore, for a  $2 \times 20$ 2064 module configuration plus 10 spares, one needs 500 kCHF. The cost of the electronics 2065 and readout will depend on the required segmentation. Since each MCP-PMT has the 2066 anode divided into 64 independent sections, the array of  $2 \times 20$  modules could provide 2067 up to 2560 channels. Assuming a very modest segmentation of each anode into only 4 2068 groups gives a total of 160 channels. The cost per channel for the current T0 electronics 2069 is  $\sim$ 4 kEUR. More units will reduce the cost per channel. The total cost of T0 Upgrade 2070 is estimated at ~1 MCHF. This sum would be equally divided between the detector units 2071 (500 kCHF) and electronics (500 kCHF). 2072

<sup>2073</sup> The preliminary cost estimate for the V0-Plus detector is:

Scintillation plastic	10,500 CHF
Optical Fibers	10,000 CHF
PMT Hamamatsu quotation 2013	10,000 CHF
Front End Electronics, Data Acquisition System, Detector Control System	130,000 CHF

Final cost estimating is underway; the numbers provided are present rough estimates The total cost of the V0-Plus as described is 500 kCHF.
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### Chapter 11

## Zero Degree Calorimeter - ZDC

#### **11.1** The present ZDC readout system

The ZDC acquisition and trigger system has been designed with a conservative ap-2080 proach. Since it is located in one of the ALICE control rooms outside of the cavern, 2081 i.e. in a zone without strong radiation levels during data taking and therefore of easy ac-2082 cess, the system uses NIM and VME electronics. At present it employs a combination of 2083 commercial and custom VME modules. The commercial modules are connected to the 2084 front-end and provide the measurement of the signal charges (CAEN V965 QDC), of the 2085 arrival time of the signals (CAEN V1290 TDC) and the measurement of their rate (CAEN 2086 V830 scalers). A custom differential discriminator has been developed for the ZDC fol-2087 lowing the idea of Refs. [70, 71] in order to provide precise triggering even in presence 2088 of low frequency noise on the baseline. The discriminated signals are combined together 2089 through standard NIM modules to provide different logical combinations that can be mod-2090 ified when changing colliding beam types. In the future the combinatorial logic will be 2091 implemented in an FPGA. 2092

Two custom modules are dedicated to the interface of the ZDC front-end with the ALICE 2093 trigger and readout systems. The ZDC Trigger Card (ZTC) alignes the ZDC trigger signals 2094 with the LHC clock and delays them in order to satisfy the timing requirements for L1 2095 triggers. The ZDC Readout Card (ZRC) is dedicated to data acquisition. Upon receiving 2096 a L0 trigger it generates a gate for the QDCs and a strobe for the TDC. At the same 2097 time a BUSY signal is sent to the ALICE Local Trigger Unit (LTU) and from there to the 2098 Central Trigger Processor (CTP). Correct timing of the ZDC signals has been achieved 2099 using delay lines. Details of the timing are given in Tab. 11.1. If a L1 trigger is received in 2100 the appropriate time window, the event is read out to the ZRC buffers otherwise the FEE 2101 buffers are cleared. At the reception of the L2 accept signal (L2a) the event is sent to the 2102 DAQ through the DDL link, while in case of a L2 reject signal (L2r) it is discarded. The 2103 present acquisition system is able to sustain a L2a rate of  $\sim 8$  kHz in the ZDC. This will 2104 double after LS1 thanks to the introduction of a Multi Event Buffer (MEB). For each event 2105

Phase	1			
ZDC signal	L0 trigger	Start	Duration	End (ns)
		(ns)	(ns)	
Collision at IP		0	0	0
Time of flight to ZDC		0	376	376
Signal formation		376	60	436
Patch cables		436	10	446
	L0 decision	0	975	975
	(LTU output)			
Cable to CR4		446	890	1336
FIFO/Cables in CR4		1336	33	1369
	L0 cable to	975	440	1415
	CR4			
	ZRC delay	1415	257	1672
	+cable			
Delay lines		1369	323	1692

Table 11.1: L0 timing for the ZDC in Run 1/2. We follow the formation and propagation of the ZDC signalsand of the L0 trigger along the different phases. The starting time for each phase, its duration and endingtime is detailed in the Table. The events are ordered according to their ending time. The delays are tuned assuch to provide a gate to the ADCs that opens 1672 ns after the collision (end of row "ZRC delay +cable")i.e. 20 ns before the arrival of the analog signal of the ZDC (end of row "Delay lines").

all the modules are readout, zero suppression is present only on the V1290 TDC. The event size for PbPb collisions is  $\sim 800$  B.

The system is controlled by a VME processor that interacts with the ALICE Experimental Control System (ECS) through the SMI protocol [72]. At the same time the processor receives some portion of the events (pushed by the ZRC) to provide calorimeter hit rate information for the luminosity monitoring. This information is made available to the experiment through the DIM protocol [73]. A detailed description of the ZDC trigger and readout system can be found in Ref. [74].

The ZDC is operated only during PbPb and pPb runs. In this way the aging of the PMTs and of the detector can be kept to an acceptable level. During p-p runs the ZDC is turned on for short periods to prepare for the ion running.

#### 2117 11.2 Upgrade strategy

#### 2118 11.2.1 Introduction

The main target of the ALICE upgrade involving the ZDC is the improvement of the readout performance, allowing to read out the detector at 100 kHz without dead time. This cannot be achieved using the current QDCs because of the fixed dead time due to the charge conversion of  $\approx 10 \,\mu$ s per event. Consequently the ZRC has to be redesigned.

#### 11.2 Upgrade strategy

<sup>2123</sup> The new ZRC will be read out by Common Readout Unit, CRU. This simplifies the design <sup>2124</sup> and gives greater flexibility.

#### 2125 11.2.2 DAQ and trigger architecture

#### 2126 Data rates

In normal operation the readout of the ZDC will be triggered by the ALICE minimum bias 2127 signal. It would be difficult to use a triggerless approach because the ZDC is sensitive 2128 also to the electromagnetic dissociation processes (EMD) that result in neutron or proton 2129 emission from the colliding ions. For PbPb collisions at LHC energies the cross sections 2130 are  $\sim 25$  times larger than the hadronic cross section since they increase faster with 2131 energy and scale as the square of the ion charge. This would result in an additional 5.2 2132 MHz event rate on the ZDC that will need to be acquired and later discarded because 2133 the other detectors are not sensitive to these events. Moreover, the V1290 TDC modules 2134 and some digitizers available on the market have a limitation to 500 kHz trigger rate. The 2135 possibility to run triggerless on events where both neutron calorimeters are hit is under 2136 investigation. In this case the contamination from EMD events is much lower, however 2137 there is a potential loss of hadronic events. 2138

For calibration purposes the system will be able to run triggerless in standalone mode. In this case a considerable dead time is induced by the saturation of the VME bandwidth because of the EMD events. However, this is not of concern because only the ZDC data will be collected.

#### 2143 Front-end readout electronics

The ZDC will replace the QDCs with digitizers with 1 GSamples/s. The modern digitizers 2144 available on the market have on-board FPGAs that allow a fast pre-processing of the data. 2145 In particular they allow integration of the signal and provide a time-stamp of arrival times. 2146 The payload of the digitizer is therefore much reduced compared to a full readout of all the 2147 samples. Another interesting feature is the measurement and subtraction of the baseline 2148 contribution to the integral. This feature allows the elimination of the modules that are 2149 dedicated to the baseline measurement, reducing therefore the payload. It would also be 2150 possible to implement pile-up rejection codes\* if the bunch spacing is reduced below 75 2151 ns. Moreover data are made available without the dead time due to charge integration and 2152 conversion typical of conventional QDCs. The new modules have large readout buffers 2153 and support readout modes faster than BLT32, up to 2eSST. The V1290 TDC modules 2154 will also be upgraded to sustain higher transfer rates with a firmware upgrade and a small 2155

<sup>\*</sup>The firmware of the flash ADC should be customised to detect the presence of another collision, that is most probably electromagnetic, in the preceding bunch crossing. Since electromagnetic pile-up affects mainly the ZDC and is difficult to detect using the information of other detectors one needs to rely only on our measurement. If another collision is present, the event could be flagged as bad or alternatively one could subtract on-the fly the pile-up contribution. As a further possibility one could write the information about the signal shape in the data to allow a more refined subtraction during reconstruction.

					Pay	load			
Source	Ch.	ADC	ADC	TDC	TDC <sup>a</sup>	ZTC	ZTC	Scaler	Scaler
		ch.	В	ch.	В	ch.	В	ch.	В
ZNA/C	5	5	40	7 <sup>b</sup>	28			3 <sup>c</sup>	12
ZPA/C	5	5	40	4 <sup>d</sup>	16			3 <sup>c</sup>	12
ZEM1/2	2	2	16	3 <sup>e</sup>	12			3 <sup>e</sup>	12
Trigger	4			4	16	4	ß	4 <sup>f</sup> +8 <sup>g</sup>	48
Control	4			3	12	1	0	3 <sup>f</sup> +1 <sup>g</sup>	16
Data		338 B					+12	24 B	
Control words		60 B					+1	2 B	
Multi hit			~80 B						
CDH+packing					60	) B			
Average			~540 B						

<sup>a</sup> Assuming a single hit per event (the multi hit contribution is accounted separately)

- <sup>b</sup> Five towers, sum of four subtowers, common && sum
- $^{\rm c}$  Common tower, sum of four subtowers, common && sum
- <sup>d</sup> Common tower, sum of four subtowers, common && sum, most exposed tower
- <sup>e</sup> ZEM1, ZEM2, OR of the two
- <sup>f</sup> V830 scaler
- <sup>g</sup> ZTC scaler

**Table 11.2:** Payload of the ZDC event, detailing the contributions of the neutron (ZNA, ZNC), proton (ZPA, ZPC) and electromagnetic calorimeters (ZEM1, ZEM2) and of the trigger and control signals. The ADC, TDC and ZTC information is readout for each event while the scalers are only readout when trigger is flagged as calibration, resulting therefore in an additional payload (as indicated). The event pile-up from the preceding and following bunch crossings results in additional payload on the multi hit TDC. This contribution has been estimated from the PbPb data taking of 2011. Space for the common data header (CDH in case it will be added by the ZRC and not by the CRU will be allocated.

hardware modification by the factory. A payload of  $\sim 600$  B per event (w.r.t. the present  $\sim 800$  B) is estimated resulting therefore in 60 MB/s at 100 kHz, making the use of VME possible (using protocols 2eVME or 2eSST). A detailed breakdown of the event payload is shown in Tab. 11.2.

#### 2160 Test of a digitizer

During the 2013 pPb data taking a test of a digitizer (CAEN V1751) in parallel to the AL-2161 ICE data acquisition was made. Its main features are: sampling frequency 1 Gsample/s, 2162 10 bit resolution, 1 Vpp dynamics, 8 channels. The signal of the common photomultiplier 2163 of the neutron calorimeter on the Pb remnant side has been sent to two channels of the 2164 V1751. In the first channel the signal has been attenuated by 4.4 dB in order to match 2165 the dynamics of the signal with the input dynamics, in the second the signal has been 2166 amplified by a factor 2 to simulate the performance of a digitizer with higher resolution 2167 ( $\sim 12$  bit). In this case only the events with low energy deposition are treated correctly, 2168 while for the higher amplitude signals saturation occurs. The digitizer was triggered by 2169

#### 11.2 Upgrade strategy

the start of LHC orbit and for each event a full orbit was recorded. The identification of the signal, the integration and baseline subtraction were performed in the offline analysis. An example is shown in Fig. 11.1. In the left plot the charge of the attenuated signal is shown and the resolution of the 1n peak signal is 26% while the resolution of the right plot for the amplified signal is 21%, closer to the value obtained with the V965 QDCs. The contribution of the 10 bit resolution is therefore significant for the attenuated signal. We will therefore need 12 bit digitizers that are just starting to be available on the market.



**Figure 11.1:** Spectra of the ZDC neutron calorimeter on the Pb-remnant side during pPb 2013 data taking at  $\sqrt{s} = 5.02 \text{ TeV}$ , obtained with a V1751 digitizer. The spectra are zoomed in the low part where the contribution of small neutron multiplicities (1n, 2n, 3n, 4n) are visible. The left figure concerns the signal attenuated by 4.4 dB, while the right figure is for the signal amplified by a factor 2. Despite that some optimization of the trigger algorithm is needed to reject noise, the spectrum for the amplified signal has better resolution.

#### 2177 Read-out board

The ZRC board will be upgraded to support the new trigger and DAQ framework. Its 2178 functionality will be similar to the present module: it will receive and dispatch L0 trigger 2179 and BUSY, will readout the front-end modules and send the data to the ALICE DAQ 2180 system via the CRU. The new board will implement faster VME cycles like VME64 or 2181 2eSST in order to have spare bandwidth on the VME bus to allow for a future increase 2182 of the luminosity and of the trigger rate. As opposed to the present ZRC that directly 2183 receives triggers on LVDS and TTC links and sends data through DDL, the new board 2184 will interface with the ALICE Common Readout Unit (CRU) that is being developed. This 2185 will simplify the design and make a future upgrade of the system easier. The connection 2186 with the CRU will be provided by one single bidirectional GBT connection. A scheme of 2187 the new ZRC board is shown in Fig. 11.2. 2188

#### 2189 Trigger and busy handling

The ZRC will receive the L0 trigger from the CRU and distribute it to the modules through NIM and ECL ports on the front panel. The trigger signal will be delayed using on-board delay chips in order to satisfy the timing requirements at the level of the front-end boards. Upon reception of a L0 physics trigger an event will be acquired on the digitizers and



Figure 11.2: Scheme of the new ZDC readout card.

on the TDC. When a calibration (software) trigger is received, the scaler modules will be read-out in addition. The events will be transferred to the ZRC and then sent to the CRU.

In case the trigger rate is high enough to saturate the transfer capability, the buffers on the front-end modules will start to fill-up and the modules will raise an "almost full" BUSY signal. The ZRC will receive these signals via dedicated inputs on the front panel and will OR them in a BUSY that is sent to the CRU. The busy is likely to occur only when the ZDC is self-triggered for calibration.

Concerning the allowed latency of the trigger signals the time of flight of the spectator 2201 nucleons, the signal formation time, the cable length and the delay lines has to be con-2202 sidered. The V1290 TDC and the digitizers employ circular memory to store temporary 2203 data that are then copied to the main buffers when a trigger is received. Since the mod-2204 ern digitizers have large on-board buffers, the limitation will be given by the V1290 TDC 2205 with its 256 word deep memory shared by each group of 8 channels. With conservative 2206 assumptions about the signal rates one can accept a L0 latency up to  $\sim 2 \, \mu s$  at the ZDC 2207 FEE (that translates into  $\sim 1.6\,\mu s$  at the CTP level) without danger of data loss. For the 2208 L1 trigger there is not a strict requirement, it will just influence the buffer size which have 2209 to be reserved for the events on the FE boards. 2210

#### 11.2 Upgrade strategy

#### 2211 Self-triggering operation

For calibration purposes the ZDC has to be readout also in self-triggering mode. The calibration run modes are:

- pedestal: to measure the baseline of the signals. This is strictly not necessary since the digitizer will offer the possibility to subtract automatically the baseline, however it will be useful as a monitoring tool to check the evolution of the baseline oscillations in different run conditions.
- laser: a light pulse is sent to the photomultipliers to measure the stability of the gain.
- cosmic ray trigger: when beam is not present, pairs of scintillators are placed above and below each calorimeter to allow triggering on the passage of cosmic rays. The light output for a minimum ionizing particle is  $\sim 1$  photoelectron and this allows the stability of the gain of the photomultipliers to be checked.
- energy calibration: a minimum bias ZDC trigger signal is used to collect a significant sample of ZDC events in a short time interval. This sample is dominated by EMD events that involve the emission of a single nucleon and therefore the calibration of the detector.
- L1 calibration: the ZDC L1 trigger inputs are used to collect a sample of selftriggered events to carefully check offline the implemented trigger logic.

For this purpose the ZRC will have NIM or ECL trigger inputs and additional trigger outputs to drive the laser pulses. Each trigger input will have a delay line to allow precise alignment with the LHC clock. Upon reception of a signal in one of the trigger inputs, if the front-end is ready and the CRU link is operational, the ZRC will dispatch the trigger signal to the front-end and forward the event data to the CRU.

In the self-triggering operation mode, depending on the beam conditions, the ZDC can
saturate the VME bandwidth and therefore have dead time. Moreover, for the pedestal,
laser and cosmic runs it will collect events that are completely uncorrelated to the rest
of the experiment. Therefore, for the moment, this operation mode is intended for standalone operation.

#### 2239 Interface to CRU

The interface with the CRU will be handled by one GBT link. The maximum theoretical VME bandwidth (320 MB/s i.e. 2.56 Gbit/s) can be actually by the GBT link.

#### 2242 **ZDC triggers**

The ZDC provides a L0 trigger given by the coincidence of the signals of the central towers of ZNA and ZNC. This reduces the background from eletromagnetic dissociation processes that is present in minimum bias triggers. This selection is routinely used in data analysis and, in this way, will be made available at L0 trigger level. The system will be based on two fast cables (one of which is already in place) connecting directly ZNA and ZNC with a trigger logic that will be placed close to the CTP.

The ZDC L1 trigger ouput is given by logical combinations of the signals of the six calorimeters. For each neutron and proton calorimeter the information has a redundancy that allows elimination of the photomultiplier noise. In the present implementation the L1 trigger logics are synchronized by the ZTC and then forwarded to the CTP using LVDS cables. The minimum latency for the ZDC L1 triggers (at the CTP input) is around 2.0 -2.2  $\mu$ s depending on the trigger logic. The use of the present approach to dispatch the L1 trigger signals will be continued.

#### **11.3 Schedule, funding and institutes**

<sup>2257</sup> The tables 11.3 and 11.4 show the schedule and funding respectively.

2014
Purchase and test in laboratory of a 12 bit ADC (R&D⇒15 k€)
Definition of the architecture of the new ZDC Readout Card
Firmware development on "evaluation board" (R&D⇒5 k€)
2015-2016
Firmware development on "evaluation board"
Design and construction of the ZRC prototype (R&D $\Rightarrow$ 30 k $\in$ )
2017-2018
Purchase of 12 bit, 1GSample/s flash ADCs (70 k€,
rough estimate assuming that the price will be half of the actual one)
Refinement of the firmware on the ZRC prototype
Test of the ZDC readout card prototype
Design and construction of two final ZDC Readout Cards (30 k€)
V1290 TDC firmware upgrade and hardware modification to allow for 2eSST cycles (5 k€)
Table 11.3: ZDC schedule

2014	20 k€ for R&D
2015-2016	30 k€ for R&D
2017-2018	105 k€ for the upgrade

Table	11.4:	ZDC	funding.
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The institutes shown below will jointly participate in the upgrade and in the testing activities:

- Sezione INFN and Dipartimento di Fisica dell'Universit, Turin, Italy
- Sezione INFN and Dipartimento di Fisica dell'Universit, Cagliari, Italy

11.3	Schedule,	funding	and	institutes
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• Gruppo Collegato INFN and Dipartimento di Scienze e Innovazione Tecnologica dell'Universit del Piemonte Orientale, Alessandria, Italy 

### Chapter 12

2264

# **Electro Magnetic Calorimeter - EMC**

#### **12.1 The EMCal detector**

The ALICE EMCal [75] is a shashlik-type sampling calorimeter that consists of ten full 2267 size super-modules (SMs) and two 1/3-size SMs, providing 107 degrees of azimuthal 2268 coverage, already installed and operated in the ALICE experiment. The EMCal coverage 2269 will be extended with six 2/3-size and two 1/3-size EMCal SMs to be installed during 2270 the 2013-2014 long shutdown of the LHC (LS1) to provide an additional 67 degrees of 2271 azimuthal coverage. A full size SM consists of 1,152 readout towers. An individual EMCal 2272 tower is read out with an avalanche photodiode and preamplifier mounted on the tower. 2273 The preamplifier signal is split into energy and trigger shaper channels on the Front End 2274 Electronics (FEE) [76] boards. The energy shaper signals are sampled at 10 MHz with 10-2275 bit resolution using the ALTRO chips [77] designed for the ALICE TPC (Time Projection 2276 Chamber) [78]. Prior to digitization, each energy signal is split into a High Gain (HG) and 2277 Low Gain (LG) channel, each shaped separately, with a gain ratio of 16 to provide an 2278 effective dynamic range of 14-bits. Each FEE board provides readout of 32 towers (HG 2279 and LG). 2280

The trigger signals of  $2 \times 2$  towers are summed and transmitted to a Trigger Region 2281 Unit (TRU) module [79] where the  $2 \times 2$  tower sums are digitized and processed in an 2282 FPGA [80]. The local high energy shower trigger decisions from each TRU are transmit-2283 ted to an EMCal Summary Trigger Unit (STU) where they are OR'ed together to form the 2284 EMCal L0 trigger. The trigger primitive data from all TRUs are transmitted to the STU 2285 upon receipt of the ALICE L0 trigger decision where the EMCal L1 single shower and 2286 jet trigger algorithms are performed. With respect to the readout system, the TRU may 2287 optionally include the trigger primitive data in the data stream, using the same format as 2288 the FEE boards. Each full EMCal SM requires 3 TRUs and 37 FEE boards, where one 2289 FEE board is used to read out reference channels of the EMCal LED-based monitoring 2290 2291 system.

The EMCal readout has been upgraded during LS1 to provide more than an order of magnitude decrease in the readout time per event, bringing the EMCal close to the ALICE post-LS2 goal of 50 kHz readout for minimum bias Pb+Pb collisions. This was achieved
 with a modification of the EMCal readout architecture using newly developed readout con centrator modules and minor modification of the existing FEE boards, and no modification
 of the TRU boards or trigger system.

#### **12.2 The EMCal readout system**

#### 2299 12.2.1 Point to point links and SRU

In the readout system used before LS1, the readout of 640 ALTRO channels within 10 2300 FEE boards on a single GTL bus took place sequentially, resulting in a minimum readout 2301 time of about 270  $\mu$ s for EMCal. After the replacement of the GTL bus with point-to-point 2302 links between the FEE boards and the readout concentrator, the FEE readout time is re-2303 duced by reading out all of the FEE boards concurrently [81]. This solution is based on the 2304 Scalable Readout Unit (SRU) developed in collaboration with the Scalable Readout Sys-2305 tem project [82] of CERN RD51. The SRU interconnects with each FEE board through a 2306 custom daughter card which was designed for the EMCal FEE board. It provides interface 2307 compatibility between the SRU and the existing EMCal FEE board to provide the Data, 2308 Trigger, Clock, and Control (DTC) links. The DTC daughter card mainly consists of an 2309 RJ45 port, an LVDS driver, and a power switching circuit. It mounts on the FEE board by 2310 making use of existing test-point holes into which pins and sockets have been inserted. 2311 allowing the DTC daughter card to be plugged onto the FEE without soldering. 2312

In order to retain compatibility with the existing ALICE online system and the off-line 2313 decoding software, and since the bandwidth of the ALICE DAQ system is not a limiting 2314 factor for the EMCal readout (see Sec. 12.2.3), the EMCal readout partition organization 2315 and its interfaces to the ALICE online system are unchanged, as illustrated in Fig. 12.1. 2316 Each SRU provides the two readout partitions of a full size EMCal SM. As described 2317 in [83], the SRU board integrates a TTCrx (LHC Trigger, Timing, and Control receiver) [84] 2318 which can receive trigger and timing information from the ALICE Trigger system. It also 2319 has three SFP+ ports directly connected to the FPGA's high speed serial transceivers for 2320 serial data transport at up to 5 Gbps. One additional SFP+ port provides a 10 GbE link. 2321 For the EMCal application, one of these transceivers is used for the Ethernet connection 2322 to the ALICE DCS system, the other two transceivers are used for the two DDL links to 2323 the ALICE DAQ system. The functionalities of the DCS and SIU boards in the previous 2324 system are implemented in the FPGA firmware of the SRU. 2325

Each SRU has 40 point-to-point links for the 40 (37 FEE + 3 TRU) boards of the two 2326 readout partitions of a full size EMCal SM. Event data, triggers, clock, and commands 2327 are transmitted over the DTC link between the SRU and each FEE board. The maximum 2328 bandwidth of a DTC link on the SRU is 2 Gbps. In the EMCal application, the bandwidth 2329 of the DTC link is conservatively limited to 20 MB/s due to the hardware capability of the 2330 rather outdated FEE FPGA (Altera ACEX 1K Family EP1k100QC208-3) and because it 2331 is sufficient to insure that the DTC link does not limit the EMCal data throughput (see 2332 Sec. 12.2.3). 2333

#### 12.2 The EMCal readout system

#### 12.2.2 Suppression of low gain readout

Each EMCal tower energy signal is split into HG and LG channel, and shaped separately 2335 with a gain ratio of 16. The LG channel data is used in the offline analysis only when 2336 the associated HG channel has saturated. The concept of the LG readout suppression 2337 algorithm is to check the HG signals in real time in the FEE FPGA and then omit the 2338 ALTRO readout of the associated LG channel if the HG signal is not saturated. For 2339 low energy signals, the HG channel information is sufficient. The EMCal offline analysis 2340 experience shows that it is very rare that the LG channels are needed. Therefore, the LG 2341 suppression readout algorithm can save readout time by eliminating entirely the readout 2342 of nearly half of the readout channels. 2343

#### 12.2.3 Implementation and test results

The above solutions have been implemented for the EMCal readout using the SRU of the CERN RD51 project, the EMCal specific DTC adapter card, and custom FPGA firmware for the FEE and SRU for the EMCal application.

Table 12.1 lists the measured average EMCal event sizes and the estimated maximum number of occupied channels in p+p and Pb+Pb collisions per readout partition. The average size of the EMCal physics events are typically less than 15 percent of the  $N_{max}$ and less than 20 percent of channels have hits in minimum bias Pb+Pb collisions.

The estimated times for each of the steps in the EMCal readout as a function of the 2352 data volume are shown in Fig. 12.2. It's seen that the ALTRO readout time ( $t_{ALTRO.32}$  = 2353  $\sim 19.3 \ \mu$ s) limits the readout rate to 52 kHz for the anticipated EMCal event sizes (see 2354 Tab. 12.1). Further improvement in the EMCal readout speed would require redesign and 2355 replacement of the EMCal FEE, at significant cost and effort. For event sizes larger than 2356 3.6 kBytes, the transmit times over the existing DDL links,  $t_{DDL}$ , will limit the maximum 2357 event readout rate (see Fig. 12.2). If necessary, this limitation can be alleviated by future 2358 firmware changes in the SRU to use the available 10 GbE link (shown as solid circles), or 2359 to upgrade the DDL link speed to 5 Gbps (both under consideration in ALICE). 2360

A plug-in DTC daughter card has been designed to preserve the compatibility with the existing EMCal hardware. During LS1, the DTC daughter cards have been mounted on all of the FEE boards and the SRU readout has been implemented and tested on all of the installed EMCal SMs. The additional EMCal SMs being installed during LS1 will be commissioned with the SRU readout.

The Low Gain readout suppression algorithm, ALTRO readout function, and the custom DTC protocol have been implemented through a FEE (and TRU) FPGA firmware upgrade. The function of the ALICE Detector Control System and DAQ Data Link boards of the previous readout system have been implemented in the FPGA firmware of the EMCal SRU to provide full compatibility with the present ALICE online system.

Full readout chain tests of the new system demonstrate a readout time of  $21.4 \ \mu s$  for EMCal event sizes expected for minimum bias Pb+Pb collisions, which may be reduced

with further fine-tuning of the firmware. While this is more than an order of magnitude 2373 improvement over the previous readout system, it is ultimately limited by the minimal 2374 read out time of the ALTRO chips (19.3  $\mu$ s) on the FEE boards. The new SRU based 2375 readout system has already been installed on the EMCal during LS1. It nearly attains the 2376 ALICE goal for the period following the 2018 shutdown to be able to record data at the 2377 anticipated 50 kHz minimum bias Pb+Pb interaction rate. The importance of multi-event 2378 buffering to keep up with the full incoming (non-uniform) event rate is shown in Fig. 12.3. 2379 With the SRU readout the EMCal can be read out either upon the receipt of the ALICE 2380 minimum bias trigger, up to almost 50 kHz, or upon rare triggers, such as the high energy 2381 shower or jet triggers provided by EMCal, which remain available unchanged with the 2382 new EMCal readout. 2383



Figure 12.1: The topology of the SRU based point-to-point readout system.

	p+p	Min. Bias Pb+Pb	Central Pb+Pb	Pedestal
N <sub>event</sub> (Bytes)	1000	2 500	5 000	35.9k
$N_{ch}$	80	220	420	1152

**Table 12.1:** The measured average size in bytes  $(N_{event})$  of various types of events, and the associated number of hit channels  $(N_{ch})$ , per readout partition of the EMCal detector. The number of hit channels is  $N_{ch} \approx (N_{event} - 68) \div 12$ , where 68 is the number of bytes of the event header and trailer; 12 is the minimum number of data bytes per hit channel.



Figure 12.2: The correlation between the readout time and the event size for the various readout steps discussed in the text.



Figure 12.3: EMCal Event rate vs Event rate for different Multi-Event Buffering values.

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### Chapter 13

# Photon Spectrometer - PHOS

13.1 The PHOS detector

The photon spectrometer PHOS is designed to detect, identify and measure with high resolution the 4-momenta of photons. Photon studies in heavy ion collisions require from the detector a high discrimination power between photons and any other kind of particles, charged and neutral hadrons or electrons.

After LS1 PHOS will have four modules, three with a full population of  $56 \times 64 = 3584 \ PbWO_4$ crystals, and a fourth module with  $\approx 1750$  crystals. The PHOS acceptance in pseudorapidity is  $|\eta| < 0.13$  and each module covers  $17.8^{\circ}$  in azimuth angle.

The  $PbWO_4$  crystal is 18 cm long with a squared cross-section of  $22 \times 22$  mm<sup>2</sup>. It provides 2394 20 units of radiation length ( $X_0 = 0.89$  cm). Its cross section is chosen to be comparable 2395 with the Molière radius of  $PbWO_4$ ,  $r_M = 20$  mm. The scintillation light, in the visible near 2396 UV-wavelength range, is read out by a  $5 \times 5$  mm<sup>2</sup> avalanche photo-diode (APD) integrated 2397 with a low-noise pre-amplifier. The calorimeter is operated at low temperature,  $-25^{\circ}$ C, 2398 stabilized to  $\pm 0.3^{\circ}$ C. This operation mode on one hand enhances the scintillation light 2399 output by a threefold factor and provides the required high and constant energy resolution 2400 even for the less energetic photons and on the other hand, keeps the noise of the APD 2401 low enough to provide a high signal to noise ratio. 2402

The PHOS readout electronics resembles very closely those from EMCAL. In fact the EM-2403 CAL FE boards were originally derived from PHOS. The basic unit in the readout chain 2404 is a FEE card (FEC) that processes and digitizes data from 32 crystals. The electron-2405 ics chain for a crystal comprises the avalanche photo diode (APD), a charged sensitive 2406 preamplifier (CSP), and an analog shaper with a band-pass filter and amplifier. The 2407 shaper delivers two semi-Gaussian energy signals with peaking time 2  $\mu$ s, one with low 2408 gain (LG) and one with high ( $\times 16$ ) gain (HG). In addition, a short energy pulse with peak-2409 ing time  $\approx$  100 ns is generated for the Trigger Region Unit (TRU). The LG and HG energy 2410 signals are digitized in four ALTRO 16-channels 10-bit ADCs, giving a 14 bit dynamic 2411

Event type	рр	PbPb min.bias	PbPb central	pedestal
Event size, kB	1.2	8	25	160
$N_{ m hits}$	8	70	220	1792

 Table 13.1: Event size and the number of hits per events in one PHOS partition in different types of events during Run 1.

range up to 100 GeV. The 32 short pulses are analog summed  $2 \times 2$  to eight signals and transmitted to the TRU.

A Read Out Branch (ROB) comprises 14 FECs and one TRU. The PHOS module with 3584 crystals includes eight ROBs with a total of 112 FECs and 8 TRUs. The module is read out by four Readout Controller Units (RCUs), each RCU controls two ROBs. (The RCU was developed for the TPC detector). The FECs and TRU of a ROB are interconnected to one of the two RCU ports by a GTL cable bus. The readout over a single GTL bus takes place sequentially.

The TRU delivers L0 triggers by searching for energy clusters in a ROB mapped to a 14  $\times$  8 matrix (14 FECs  $\times$  8 signals). The PHOS TRU digitizes the quad analog sums in 20 MHz ADCs. A parallel search over all 112 of the 4  $\times$  4 windows are carried out by the the FPGA firmware. The L0 energy threshold is programmable. The trigger outputs from all TRUs are ORed in a Trigger OR (TOR) device. The TOR can also be programmed to deliver L1.

The PHOS electronics, with the exception of the readout units, are contained inside a gas tight volume. The FEC and TRU boards are mounted inside water cooled copper boxes. To prevent condensation of humidity inside the electronics compartment the volume is filled with nitrogen. The RCUs are mounted on the bottom shield of the module.

The average event size and the number of hits per event for pp, minimum bias PbPb and central PbPb collisions, as well as for pedestal runs without zero suppression, were obtained from data taken during Run 1. These values for one readout partition and the maximum of 64 time samples are collected in the Tab. 13.1. Note that data of pedestal runs contains all 64 time samples in all high- and low-gain channels, while in physics runs with zero suppression the high-gain channels dominate.

#### **13.2 The PHOS readout system**

<sup>2437</sup> The target for the upgrade is a PHOS readout time of  $\approx 20 \ \mu s$  to match a 50 kHz inter-<sup>2438</sup> action rate in PbPb collisions. This requires a point-to-point readout topology such that <sup>2439</sup> all FECs can be read out in parallel. PHOS has therefore adopted the SRU DTC point-<sup>2440</sup> to-point links installed for EMCal and DCal as described in the previous section. In [85] <sup>2441</sup> EMCal quotes a readout time of 21.4  $\mu s$  measured for event sizes expected for minimum <sup>2442</sup> bias PbPb collisions. However, the data volume per ALTRO channel for PHOS is currently <sup>2443</sup> 64 time samples at 10 MHz compared with 15 time samples for EMCal.

#### 13.2 The PHOS readout system

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For the SRU system the effective readout time for a given event size is determined by
the largest transaction delay from i) ALTRO bus, ii) DTC link between FEC and SRU, and
iii) the digital data link (DDL) between SRU and the DAQ system. This is illustrated in
Fig. 13.1. The readout time can be minimized by 1) reducing the number of time bins,
limiting the data volume from SRU to DAQ by using fewer DTC links, and 3) using two
DDLs instead of one.



Figure 13.1: Calculated readout times for PHOS SRU configuration. Up to 9 kB/SRU the time is dominated by the ALTRO protocol. Note that the individual contributions from ALTRO, DTC and DDL are not additive.

<sup>2450</sup> Calculations [86] show that the minimum ALTRO readout time with 64 time bins is around <sup>2451</sup> 25  $\mu$ s. This value is reduced to  $\approx$  20  $\mu$ s and  $\approx$  18  $\mu$ s for 32 and 16 time bins, respectively. <sup>2452</sup> However, the current 64 time samples can safely be reduced to 32 because it is sufficient <sup>2453</sup> to sample the first  $\approx$  3.2  $\mu$ s of the pulse which will cover both its rising edge and the <sup>2454</sup> maximum amplitude.

To switch to 16 time samples would require a shorter pulse from the analog shaper by changing the shaping time constant from  $2 \mu s$  to  $1 \mu s$ . This will have a negligible effect on the energy resolution. However, it would require a major intervention by changing a very large number of capacitors on the FECs.

Shortening the pulse length will reduce the probability of pileup in a channel. However, as shown in [87] the mean time between hits in a cell for an average PbPb event is  $\approx$  400  $\mu$ s. With proper timing calibration, all cells can be aligned within 3 ns. It will therefore not be a problem to identify data from BCs with 25 ns spacing. Pileup effects can therefore be neglected also with the current pulse length. The event size after the change to 32 time samples will be roughly half of that shown in Tab. 13.1.

The performance of the chosen topology is shown in Fig. 13.1, with 4 SRUs per PHOS module and using 30 out of the 40 DTC SRU links. The SRU and FEC firmware are optimized for 32 time samples per channel with Low Gain readout suppression algorithm [86]. For an event size of 8 kB/SRU, corresponding to  $\approx$  110 kB for the full PHOS detector, the theoretical readout time is 22  $\mu$ s giving a maximum rate of around 45 kHz. The readout topology of one PHOS module is schematically shown in Fig. 13.2.



Figure 13.2: Readout and trigger topology of the PHOS modules M2, M3 and M4. The dashed rectangle contains the FE electronics inside the module.

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### 2472 13.3 Possible improvement of photon identification

One of the main physics goals of PHOS is the measurement of direct thermal photons.
This is the only way to determine the initial temperature of the hot fireball created in high
energy heavy-ion collisions at LHC.

According to the theoretical estimation [88] and preliminary measurements by ALICE [89, 90], the thermal photon signal in central PbPb collisions at LHC is to be searched for in a rather narrow  $p_T$  range of 1-10 GeV/*c*, and the expected excess of direct photons over background decay photons is as small as 5-10%.

#### 13.3 Possible improvement of photon identification

The measurement of the thermal photons is a quite difficult and challenging task, since 2480 their expected signal is rather weak (a few per cent) as compared to a high physical back-2481 ground of decay photons from hadrons produced in the same collision. Moreover, since 2482 any electromagnetic calorimeter is sensitive not only to photons, but also to charged and 2483 neutral hadrons, the photon spectrum to be measured by PHOS at LHC is contaminated 2484 by all these signals. Preliminary studies of direct photons in PbPb collisions taken by 2485 the PHOS spectrometer in 2010 [90] show that systematic uncertainty from hadron con-2486 tamination dominates in central collisions. It can be illustrated by Fig. 13.3, which shows 2487 a systematic uncertainty from hadron contamination at the level of 3-7 % at centralities 2488 0-10 % in the that  $p_T$  range where the direct photon signal is expected. Such system-



Figure 13.3: Systematic uncertainties of direct photon spectrum in central PbPb collisions measured by PHOS.

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atic uncertainty is still large and comparable with expected direct photon excess over
 background. Further reduction of this systematic uncertainty is possible only by stronger
 suppression of hadron contamination of the photon spectrum.

Photon identification in PHOS has been provided by two criteria: anti-matching of PHOS
clusters with charged tracks selects neural particles, and cluster shape analysis discriminates showers developed in PHOS by electromagnetic particles (photons and electrons)
from hadrons. According to the experience of the PHENIX experiment at RHIC, cut on
arrival time was very useful in direct photon measurement, and the timing cut was always
used in measurements of direct photon spectra [91].

The challenges in identifying thermal photons in the high background from decay photons plus signals from charged and neutral hadrons are discussed in [92]. Adding timing cut to other photon identification criteria improves hadron suppression, especially from neutrons and anti-neutrons, as illustrated in Fig. 13.4.

<sup>2503</sup> Depending on the time resolution, discrimination against hadrons by cluster timing is <sup>2504</sup> effective up to  $\approx$  2-3 GeV. To add significantly to the discrimination power, the resolution <sup>2505</sup> should be 1 ns or better at the cluster energy E = 1.5 GeV. Using pulse shape analysis in <sup>2506</sup> the time domain a resolution of  $\approx$  1.5 ns has been measured in the lab, whereas  $\approx$  3 ns has been obtained from data from Run 1. At the same time, test beam measurements [93] show that the intrinsic time resolution with PWO crystals is  $\approx$  0.5 ns at 1.5 GeV.

To reach a value better than 1 ns will require a change of the frontend electronics. Preliminary studies have identified a possible solution based on adding a timing daughter card to the FEC. A feasibility study of such an upgrade implementation for LS2 is under way.



Figure 13.4: Improvement of discrimination against hadrons with cluster timing.

### Chapter 14

# High Momentum Particle Identification Detector - HMP

#### 2515 14.1 Introduction

The ALICE High Momentum Charged Particle Identification Detector (HMP) performs 2516 charged particle identification by means of the measurement of the Cherenkov angle, 2517 exploiting the momentum information provided by the tracking devices. It consists of 2518 seven identical proximity focusing Ring Imaging Cherenkov (RICH) counters. The HMP is 2519 able to provide 3 sigma separation for  $\pi/K$  in the momentum range 1 GeV/c < p < 3 GeV/c 2520 and in the range 1.5 GeV/c GeV/c for K/p that, at 2 sigma, can be pushed up to2521 6 GeV/c. The radiator used is  $C_6F_{14}$  (n = 1.2989 @ 175 nm,  $\beta_{th}$  = 0.77), 15 mm thick. 2522 The photon detection is provided by multiwire chambers coupled with pad-segmented CsI 2523 photo-cathodes (CsI Q.E.  $\approx$  25% @ 175 nm, pads size 0.8x0.84 cm<sup>2</sup>). The amplification 2524 gas is CH4 at atmospheric pressure, the anode-cathode gap is 2 mm and the operational 2525 voltage is 2050 V (gain  $\approx 4 \times 10^4$ ). The 42 photo-cathodes are segmented in 3840 pads 2526 each with individual analogue readout. The front-end electronics (FEE) and Readout 2527 (RO) are based on GASSIPLEX and DILOGIC chips, both developed within the HMPID 2528 project. The noise level is 1 ADC channel (1000 e-) whereas a single photon signal 2529 amplitude is of the order of 30 ADC channels on average. Lesss than 200 out of 161280 2530 channels are dead or noisy. A detailed description of the detector can be found in [94]. 2531 HMP has successfully collected pp, pPb and PbPb data during the LHC operation period 2532 Run 1 and it has contributed as expected to the physics program measuring charged 2533 hadron spectra and ratios. The same conditions of operation are planned for the HMP 2534 during the Run 2 period, when the LHC will increase the collision energy. 2535

After the ALICE upgrade the HMP will be able to exploit its maximum event read out rate of 2.5 kHz in central PbPb collisions, with an increasing factor of 4 w.r.t. Run 1 and Run periods, when the drift time and the TPCread-out rate imposed lower rates. No CsI Q.E. degradation is expected for the upgrade operation since the estimated charge dose of 0.16 mC/cm<sup>2</sup> will be less than 0.2 mC/cm<sup>2</sup>, which is the threshold considered where

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possible ageing effects of CsI could be observed [95, 96]. With the increase of the readout rate, the HMPID will have an event statistic higher w.r.t. to Run 1 and 2. Thus it will
provide in shorter time the PID measurements for the planned physics and calibration
points for the TPC, that uses the dE/dx PID, down to 4 GeV/c (minimum of the specific
ionization energy loss).

### 2546 14.2 Implementation architecture

The full exploitation of the HMP read-out rate at 2.5 kHz for central PbPb collisions ensures the PID for the defined upgrade physics program. No upgrade of the electronics is planned. The detector can be easily integrated in the ALICE read-out architecture as the upgraded ALICE system provides backward compatibility.

Each HMP module is read out by two optical links, on for for each module side (Fig. 14.1). On each side the electronics is organised in 24 columns, with 10 front-end Gassiplex cards per column. Each Gassiplex card is equipped with 3 Gassiplex chips and the DILOGIC chip for a total of 48 channels and connected to a Multi-Chip-Module that provides channel multiplexing, ADC conversion and zero suppression. Upon L0 arrival the 24 columns are read out in parallel and the content is transferred in the column memory buffers. The L0 latency that optimizes the peaking time is 1.2  $\mu$ s.



Figure 14.1: Schematics of the implementation of the FE and readout electronics on one HMPID module.

<sup>2558</sup> Due to the relatively smooth bell shape of the shaping preamplifier, an increase of 50% of <sup>2559</sup> latency brings the signal loss to 30% whereas an increase of only 100 ns of latency would <sup>2560</sup> bring the signal loss at  $\approx$  10%. The corresponding degradation of the Cherenkov angle <sup>2561</sup> resolution for a 50% of signal loss is 12% [97]. Upon L1 signal arrival the 24 columns

are sequentially read out and the data are sent via DDL 1 to the DAQ. Extrapolating 2562 the results from Run 1 in central PbPb collisions @ 5.5 GeV at the full read out rate 25 2563 kB/s data rate is expected. The trigger signal management is ensured by cables and the 2564 standard TTCrx card, connected to the LTU via optical fibres. The full detector operation 2565 is ensured by: 14 DDL 1 optical links, 14 RORC1 cards, 14 TTCrx cards, 14 L0 cables 2566 and 14 busy cables. For the debugging of trigger timing, one TTCit board is planned to 2567 be added. In conclusion, the HMP can take data in the upgraded system maintaining 2568 unchanged its read-out and trigger electronics. 2569

### Chapter 15

# Alice Cosmic Ray Detector - ACO

The Alice Cosmic Ray Detector (ACO) produces a L0 input trigger signal to the ALICE CTP and provide precise information on cosmic rays

ACO consist of an array of scintillator plastic counters placed on the top sides of the 2574 ALICE magnet. The current layout of the cosmic trigger on the top face of the ALICE 2575 magnet consists of 60 scintillator modules arranged in a doublet configuration. Each 2576 doublet consists of two superimposed scintillator counters and contains one front-end 2577 electronics (FEE). The signal of each of the two scintillators contained in one ACO module 2578 is applied to a leading edge discriminator and the FEE provides the coincidence signal of 2579 one ACO module from the two signals coming from the two scintillators, see Fig. 15.1. All 2580 the modules are connected to the main electronics card which processes the information 2581 to generate a single muon and multi muon trigger signals (see Fig. 15.2). 2582

The ACO main card receives the 120 differential signals coming from the 60 FEE cards. These signals are translated to CMOS levels and sent an ALTERA FPGA. The Cosmic trigger signal is generated by combinational logic. The TTS interface is a TTC protocol. ACO is read out via an DDL1 interface (see Fig. 15.3).



Figure 15.1: ACORDE FEE Diagram.

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Figure 15.2: Diagram of the 60 modules connected to the main card.



Figure 15.3: Block diagram of the ACORDE main card.

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### **Chapter 16**

# **Cost summary**

Table 16.1 summarises the system upgrade cost. The numbers contain electronics upgrades, fiber installation and if applicable the CRU and DDL3 fibers. They are excluding the active components in the DAQ side DDL3 interface. Main uncertainties arise from the estimate of fiber installation cost.

Detector	system upgrade cost [kCHF]
MCH	2806
MID	660
ZDC	194
TOF	750
FIT	1500
TRD	419
EMC	0
РНО	200
HMP	0
CTP	188
Total	6717

Table 16.1: System upgrade cost overview

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