CAM Test Guide

Contents:

Module set-up for CPLD programming & JTAG/BS access

Module Testing (Post JTAG)

http://www.ep.ph.bham.ac.uk/user/staley/CAM/CAM_Test_Guide.pdf
Fibre Optic Transmitters

There are three SFP modules but only U3 Transmitter has a connection to the power supply. These modules use a Class1 Laser and are safe under normal conditions. However, being SFP style, they may be removed during the JTAG testing.

Pre-Power checks

Original Heatsink on VR1 is too large and must be removed. A suitable replacement is part# 170-073 from Farnell.

Check for shorts across power rails to ground. Take ground connection from the central power connector, or a nearby ground-bar. (see below for layout)

- 5V_in and 3V_in - use power connector
- VCC3V3 plane - LK21 or TP23
- VCC_PECL plane - LK20 or TP24
- VCC_SPARE - LK19
- VCC_ADC - TP22

Initial Power-up checks

Check front-panel supply indicators D1 & D2 are lit.

Check outputs of onboard regulators measure as follows:

- VCC3V3  TP23  3.3V +/- 10%
- VCC_ADC  TP22  3.3V +/- 10%
Module configuration for JTAG access & BS testing.

There are no links specific to JTAG testing that need adding. The single JTAG chain is accessed through the 10pin front panel connector which has a pinout for the ALTERA ByteBlaster cable.

JTAG checks

Connect Byteblaster compatible cable to PL1 and using Altera Quartus programming software scan for the following JTAG devices:

   1st    EPM3256A
   2nd    EPM3032A

If all present, program devices with the following files.

   EPM3256A   …cam/vme/vme_control.pof
   EPM3032A   …cam/ttc/ab_decoder.pof

(Power down)

Boundary Scan (BS) testing

Not relevant here as the JTAG/BS access/coverage is very limited. The ECL devices in the clock paths do not have JTAG/BS ports, and adding this function would increase the complexity of the circuit and degrade the timing performance.

Module Bench Testing (Post JTAG programming)

The CPLD firmware contains test functions that allow bench testing without VME connected.

The test modes are enabled using links PL3, PL4 and PL5, and will be set as described in the tests that follow after this section.
Switch/Multiplexer test functions:

<table>
<thead>
<tr>
<th>MuxTest mode</th>
<th>Test Links PL5, PL4</th>
<th>Reference clock select</th>
<th>Variable clock select</th>
<th>Fibre Tx</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0, 0</td>
<td>Normal / VME</td>
<td>Normal / VME</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>0, 1</td>
<td>Count</td>
<td>Counter</td>
<td>ON</td>
</tr>
<tr>
<td>2</td>
<td>1, 0</td>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>3</td>
<td>1, 1</td>
<td>0</td>
<td>1</td>
<td>Off</td>
</tr>
</tbody>
</table>

ADC test functions:

<table>
<thead>
<tr>
<th>ADCTest mode</th>
<th>Test Links PL3</th>
<th>ADC access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal / VME</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Continuous</td>
</tr>
</tbody>
</table>

Ensure a link has been fitted in the supply feed, from LK20 to LK21, to power the PECL devices.

Test Procedure

(1) Voltages and clocks

Power-up and check for the following:

$$VCC_{PECL} \ (TP24) \approx 3.3V$$

TP10 has a 15us clock
(2) Input Multiplexers

Method: Apply clock signal to each input (C0i ... C15i) in turn while monitoring selected test point with oscilloscope. (Input sensitivity 100mV p-p, recommended level > 400mV p-p)

Link PL4 to place VME CPLD in test mode ‘1’ which continuously selects each input in turn to produce a multiplexed signal with a timeslot duration of 15us.

Trigger ‘scope from TP14 (TEST1) (TP1 = Ground for high-speed probe if needed)

- Probe TP3 (Refclk) for ClockA selection
- Probe TP2 (Varclk) for ClockB selection.

For example, a signal applied to clock input 2 (C2i) will appear in the second timeslot from the trigger pulse:
(3) Fibre Loop-back tests

With multiplexers still in test mode ‘1’, apply TTC signal to backplane connector. Trigger ‘scope from TP14.

- Probe TP2 for selection.

Connect fibre from Tx1 to Rx1 and check TP2 for activity in the timeslot shown below. Repeat for the fibre reconnected to Rx2, then to Rx3.

For example, with a fibre connected to Rx1 to waveform should be similar to:

![Waveform Diagram]

(4) Phase Detector

Place module in test mode ‘3’, ie link PL4 and PL5. Apply two 40MHz clocks offset by ≈ 1kHz and observe a sawtooth on TP4 – ADC input

Applying 40MHz to Input 0 (C0i), and 40 + Δf MHz to Input 1 (C1i) gives the following waveform on TP4. (The period of the sawtooth is 1 / Δf )

![Waveform Diagram]
(5) ADC control

Link PL3 for ADC TestMode to force continuous readout cycles from ADC.

- Probe TP11 and TP13

Check signals on TP11 (ADC_cs*) and TP13 (ADC_SCLK) confirm to those below. (Use TP11 to trigger the oscilloscope).

- Probe TP11 and TP12

Checking TP12 ADC_DATA will show a burst of data similar to the figure below. The actual logic values will be different, but the timing structure will be similar.
(6) BogusTTCrx

Apply TTC signal to backplane connector

Check for 80MHz and 40MHz clocks on SK17 (front panel Dual-Lemo)

If above OK then Probe:

TP7 CHA_B_CPLD for 40MHz  
TP5 VIOLation for logic0  
TP6 NRZ80 for 40MHz

Configuring for VME Testing

Set Serial number using solder-blob links. Binary# with SB1 = msb. A blob = ‘1’

Note: Production modules are numbered from 3 upwards.

Apply sticker with serial number.

VME Testing

Covered elsewhere, but will include the following tasks:

Read ID Register and Serial number Register

Write/read Control and Mux Select Registers

Apply 40MHz clock and set both muxes to select this same clock.  
Check the ADC returns a value near ½ FSD, ie 200h
Front panel layout
### Backplane lower connector pinout

#### Connector 3 (292-336mm) Type B-22 connector

<table>
<thead>
<tr>
<th>Pos.</th>
<th>E</th>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>&lt;G&gt;</td>
<td>&lt;G&gt;</td>
<td>&lt;G&gt;</td>
<td>&lt;G&gt;</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>&lt;G&gt;</td>
<td>TTC+</td>
<td>&lt;G&gt;</td>
<td>CAN+</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>&lt;G&gt;</td>
<td>TTC-</td>
<td>&lt;G&gt;</td>
<td>CAN-</td>
<td></td>
</tr>
</tbody>
</table>

#### Connector 4 (336-361mm) Type D (N) connector

<table>
<thead>
<tr>
<th>Pos.</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>+3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Power GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>+5.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Diagram of connector pinout](image-url)