CPM (v2.0) User Guide
(PC3189M/4)

Module set-up for JTAG/BS testing.

Contents:

Changes from /3 to /4 PCB
Check for Supply Shorts
Fitting Heatsinks
Fibre-optic Transmitters
Wiring Modifications for BS testing
Module Configuration for JTAG access.
LVDS receivers (optional)
Power-up Voltage Checks

http://www.ep.ph.bham.ac.uk/user/staley/CPM4_JTAG.pdf
Changes from /3 to /4 PCB

Signal DS* on CPLD U7 pin100 is now driven by a buffer that cannot be disabled.

Pin AL17 on the CP chips (U183, 171, 149, 120, 92, 63, 38, 12) is now driven by the clock distribution PLLs. If desired, the clock signals can be controlled by signals JTAG_PLL_TEST and JTAG_CLK40 if PL28 is linked. (Remember unpredictable behaviour of PLL CY7B9950 in TEST mode.)

FLASH memories supply now hardwired into PCB using etched links.

CAN uC configuration switch bank replaced by link + IC.

Minor changes in the netlist concerning clock terminating resistors.
Supply Shorts

Check for shorts across power rails to ground. Take ground connection from the central power connector, or a nearby ground-bar. (see below for layout)

- 5V_in and 3V_in - power connector
- VCC3V3 plane - TP118
- VCC2V5 plane - TP119
- VCC1V8 plane - TP83

Fibre Optic Transmitters

Although these are Class1 LASERS and are safe under normal conditions, if fitted, they may be powered-off during JTAG testing by removing the supply link from PL8. LED DS1 indicates that the modules are powered.

Heatsinks.

G-Link parts U8 and U30 must be fitted with heatsinks (Wakefield 62435ABT4).

When fitting heatsinks, please ensure U8’s heatsink is in contact with TR2 using a spot of thermally conductive paste. Likewise for U30 and TR4 as shown below:

![Heatsink Diagram]

At this stage, the large XILINX FPGAs will not be configured and so do not require heatsinks.

Can uC

Ensure PL64 is open.
Module configuration for JTAG access & BS testing.

- Ensure all three JTAG headers have their polarising pins cropped.
  Pins 5 & 8 of PL14, PL56 & PL61.

These headers are for a Xchecker connector.

- Configure JTAG chain #1 on PL56
  Ensure PL55 block has no links

- Configure JTAG chain #2 on PL61
  Ensure PL60 block has no links

- Configure JTAG chain #3 on PL14
  Ensure PL12 block has no links, and TTCdec removed from SK10 / 11.
  Also ensure that:
  PL26 fitted. (TTCDec JTAG data bypass)
  PL41 & PL24 fitted. (ALTERA feeding TTC) & (TTC feeding Xilinx)
  PL23 open. (Feed into XILINX chain.)
  PL15 fitted,(feed into ALTERA chain)
  PL19 fitted (read from XILINX chain)
  PL20 open (read from ALTERA chain)
  PL17 & PL18 fitted (TMS feed)
FLASH and FIFO supply options.

No action necessary. The default settings are now hardwired. Etched links and solder-bridges are still available in the unlikely event these have to be changed.

ROCs and HITSUM Configuration jumpers

No action necessary. The default settings are now hardwired. Etched links and solder-bridges are still available in the unlikely event these have to be changed.

Clock distribution

The following scheme allows the 40MHz clock tree to be driven by the JTAG tester software. The 40MHz PLL buffers are set to a test/bypass mode.

Remove TTCdec module if present.

Link PL28 and PL31 to drive clock tree (U74, U79 etc) from U7 pin 138 (JTAG_CLK40).

PLL inside U20 will be bypassed when U7pin136 (JTAG_PLL_TEST*) is driven low.

PLLs inside U59, U139, U192, U148, U91 and U37 will be ‘bypassed’ when U7pin137 (JTAG_PLL_TEST) is driven high. NOTE that the CY7B9950 part in TEST MODE behaves differently from expected in that some outputs may appear inverted after a number of clock cycles.

Ensure PL33 is left open to disconnect onboard oscillator.

LVDS receivers (These packages do not have JTAG access, so additional test hardware is needed, which is still under development)

Vref Nets

These pins on the CP FPGA are biased near their threshold voltage from a low-current driver (LP2996) having a typical output impedance of 2.5kohms at ±30uA. This signal may be over-ridden using one of the connected FPGA pins to drive a full logic swing.
Power-up Voltage checks

Plug in and power-up. Check front-panel voltage indicators are on.

Check outputs of onboard switchers and regulators measure as follows:

<table>
<thead>
<tr>
<th>Supply</th>
<th>Test Point</th>
<th>Measured V on PCB #7</th>
<th>Expected range</th>
<th>1/R factor</th>
<th>Rated value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC3V3</td>
<td>TP118 - TP115</td>
<td>3.3V +/- 10%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC2V5</td>
<td>TP119 - TP116</td>
<td>2.5V +/- 10%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC1V8</td>
<td>TP83 – TP80</td>
<td>1.8V +/- 5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT0</td>
<td>TP102 - GroundBar</td>
<td>1.25V +/- 20%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT1</td>
<td>TP98 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT2</td>
<td>TP78 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT3</td>
<td>TP46 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT4</td>
<td>TP18 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT5</td>
<td>TP3 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC_AN</td>
<td>TP119 - LK?</td>
<td>3.3V +/- 10% (if powered)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref0</td>
<td>TP105 - GroundBar</td>
<td>1.25V +/- 20%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref1</td>
<td>TP101 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref2</td>
<td>TP79 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref3</td>
<td>TP47 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref4</td>
<td>TP19 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref5</td>
<td>TP12 - GroundBar</td>
<td>&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Current Monitoring points

The output current of each Power Module is converted to a ground referenced voltage for easy measurement. A shunt resistor plus amplifier define the 1/R conversion factor.

Location of Voltage test-points

(To be drawn)
Front panel layout

Clock
Monitor

DAQ Tx

ROI Tx

LVDS, Fibre
A, Zsync
S, CP
S, 0, 9 (VSS)
MH, ME
BH, HE
SH, GE
FH, FE
EH, EE
DH, DE
CH, CE
BH, BE
AH, AE
VI, VE

B, G
F, E
D, C
B, A
15, 14
13, 12
11, 10
9, 8
7, 6
5, 4
3, 2
1, 0
DAQ, ROI

VME, L1A

5.0V, 3.3V
2.5V, 1.8V
CAN Tx, Rx

Breakout

JTAG Access